FIG. 1

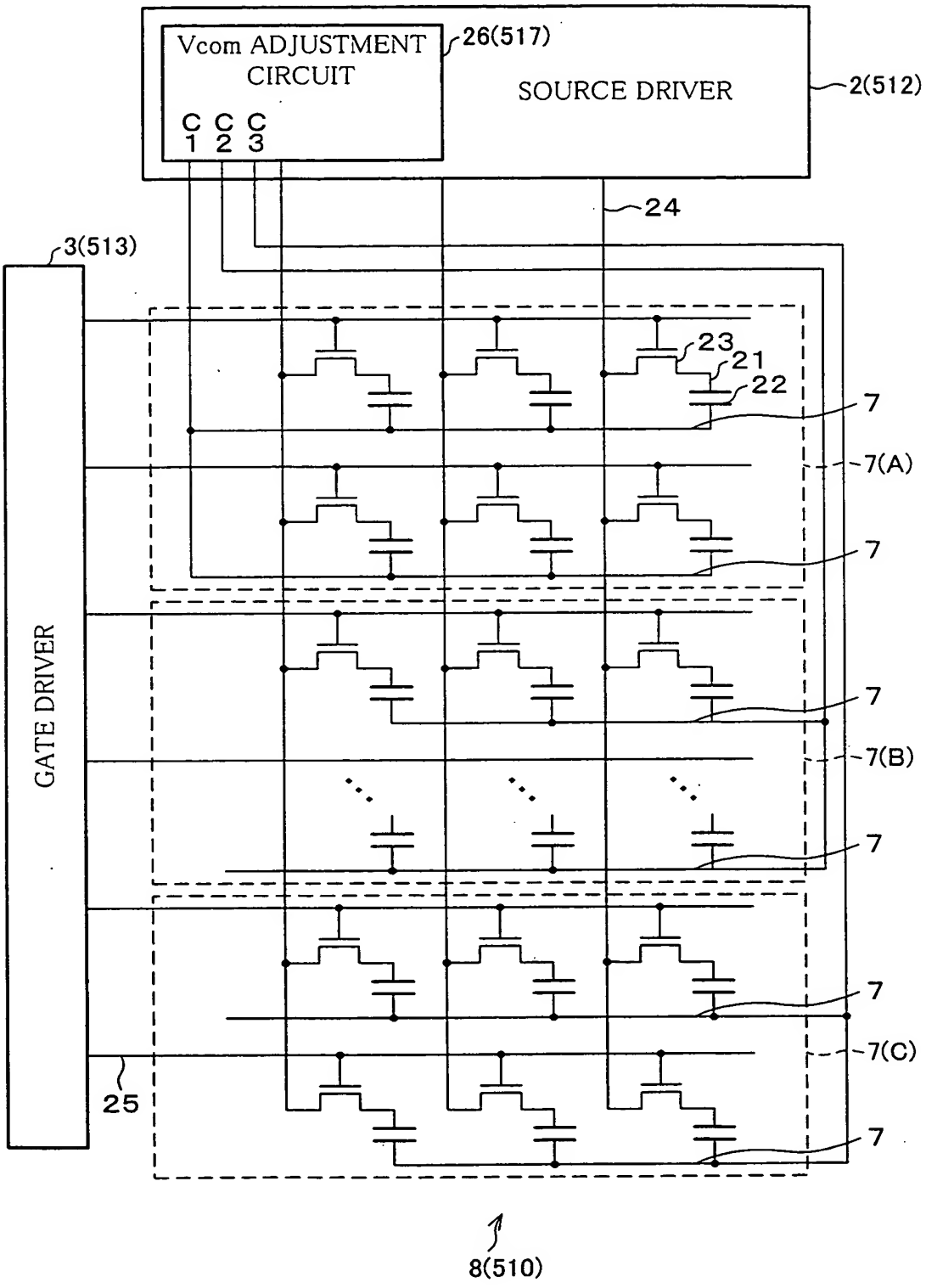

Vcom ADJUSTMENT CIRCUIT
26(517)
SOURCE DRIVER
2(512)
C 1
C 2
C 3
24
3(513)
GATE DRIVER
23
21
22
7
7(A)
7
7
7(B)
7
7
7(C)
7
25
8(510)

FIG. 2

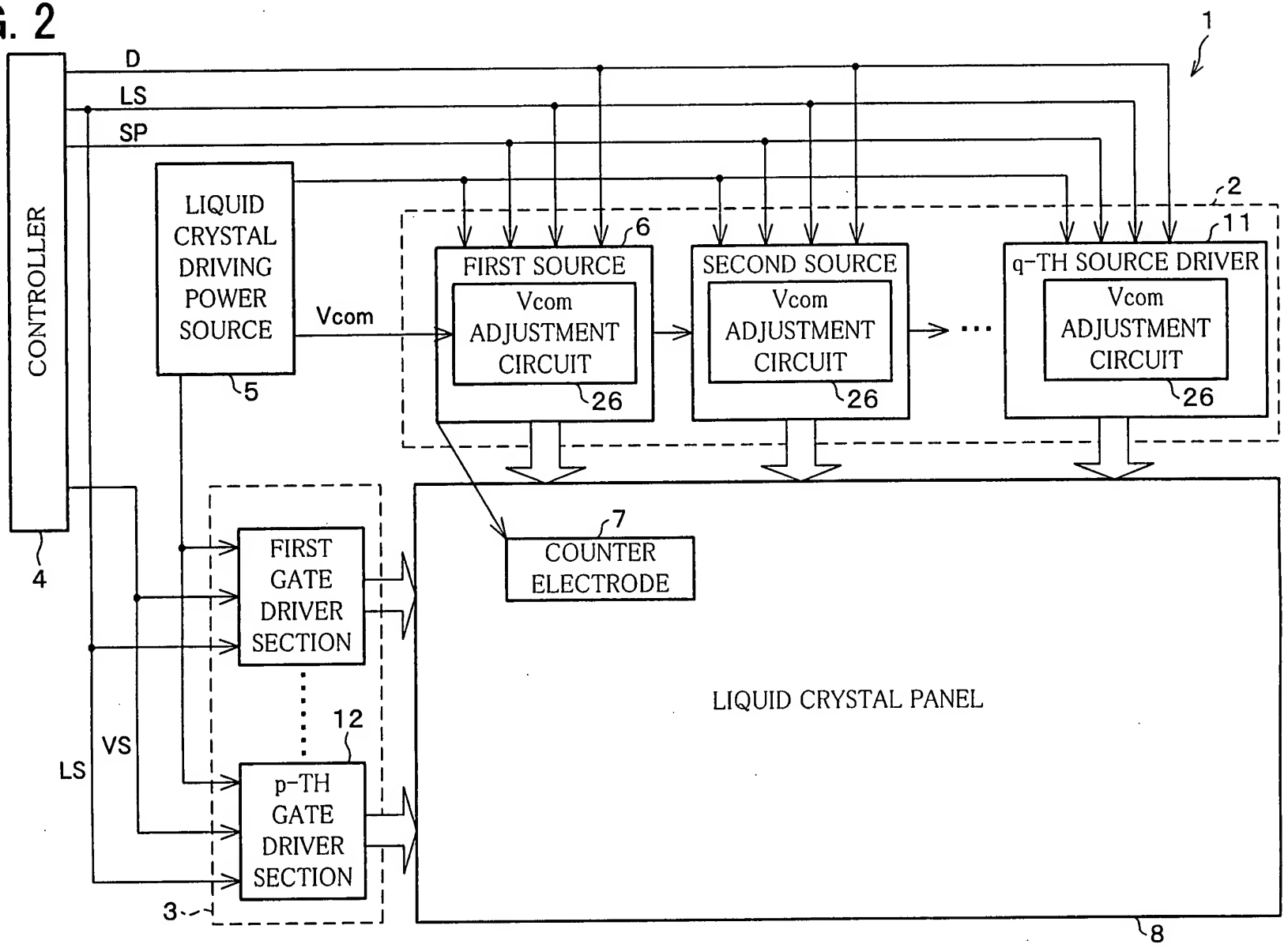

1
D
LS
SP
CONTROLLER
4
LIQUID CRYSTAL DRIVING POWER SOURCE
5
Vcom
2
6
FIRST SOURCE
Vcom ADJUSTMENT CIRCUIT
26
SECOND SOURCE
Vcom ADJUSTMENT CIRCUIT
26
11
q-TH SOURCE DRIVER
Vcom ADJUSTMENT CIRCUIT
26
7
COUNTER ELECTRODE
FIRST GATE DRIVER SECTION
12
p-TH GATE DRIVER SECTION
3
VS
LS
LIQUID CRYSTAL PANEL
8

FIG. 3

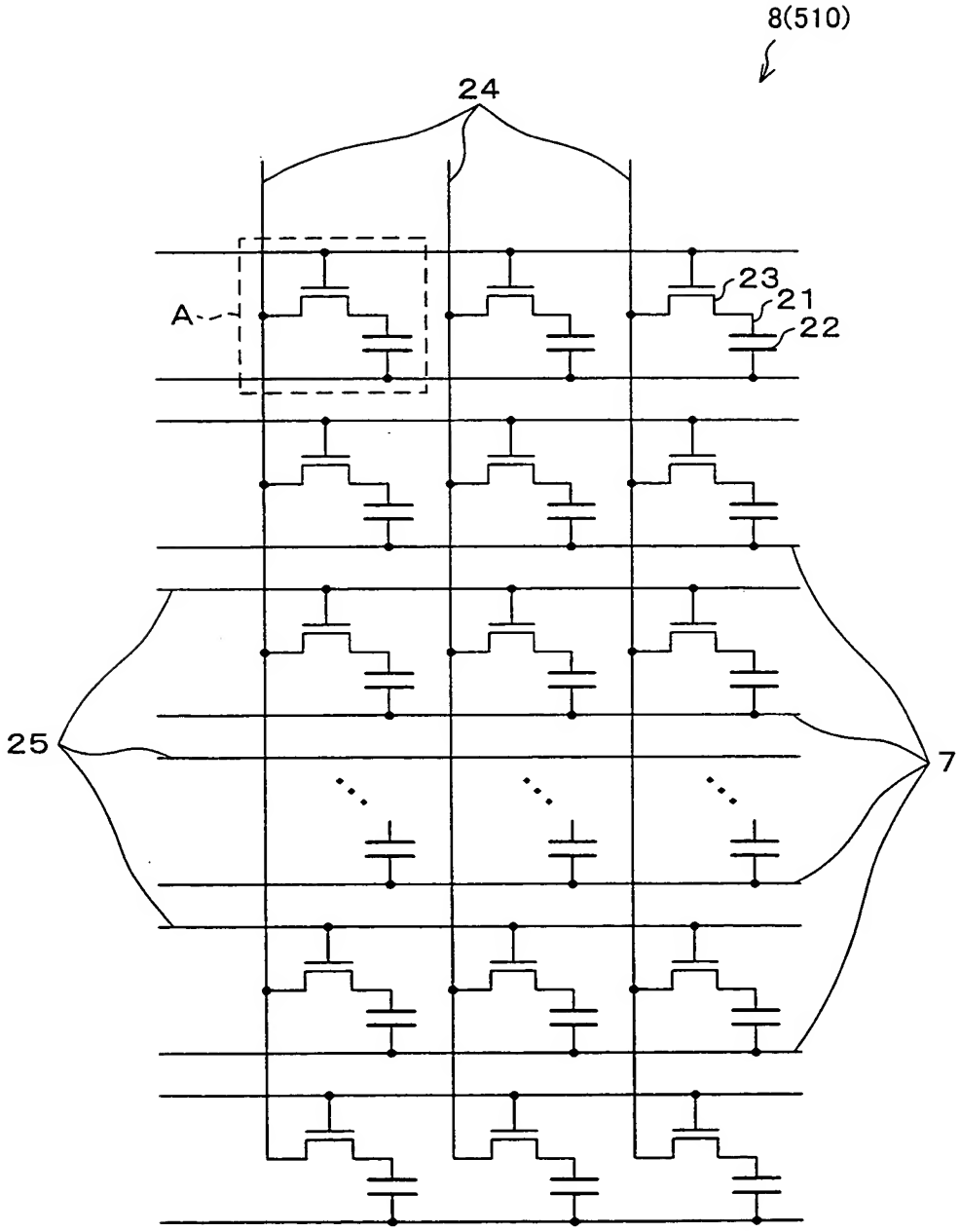


FIG. 4

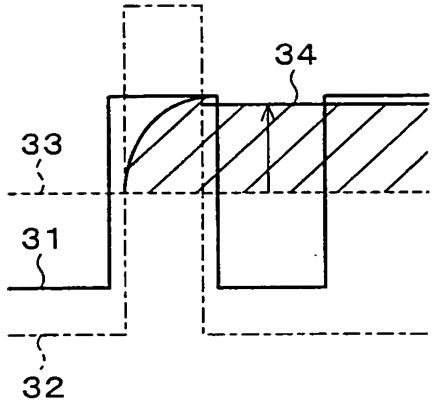


FIG. 5

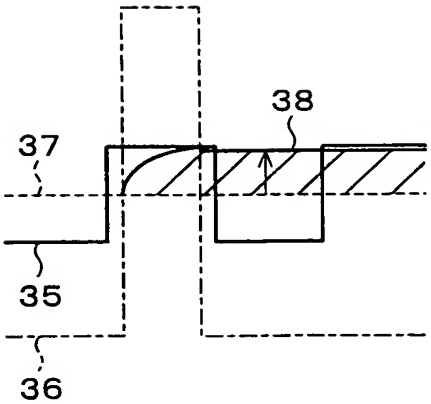


FIG. 6

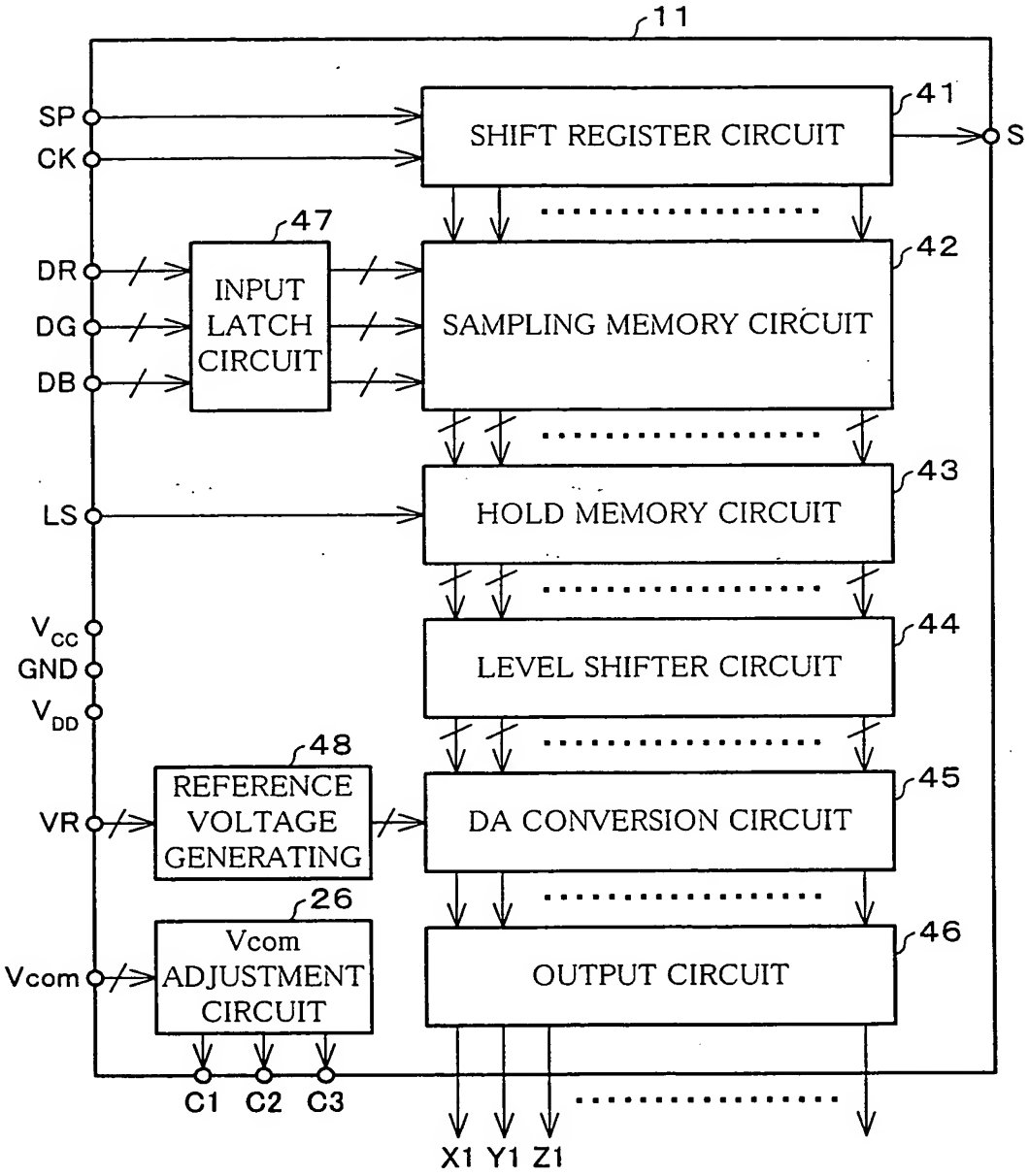

11
SP
CK
SHIFT REGISTER CIRCUIT
41
S
47
DR
DG
DB
INPUT LATCH CIRCUIT
SAMPLING MEMORY CIRCUIT
42
LS
HOLD MEMORY CIRCUIT
43
V_{CC}
GND
V_{DD}
LEVEL SHIFTER CIRCUIT
44
48
VR
REFERENCE VOLTAGE GENERATING
DA CONVERSION CIRCUIT
45
26
Vcom
Vcom ADJUSTMENT CIRCUIT
OUTPUT CIRCUIT
46
C1 C2 C3
X1 Y1 Z1

FIG. 7

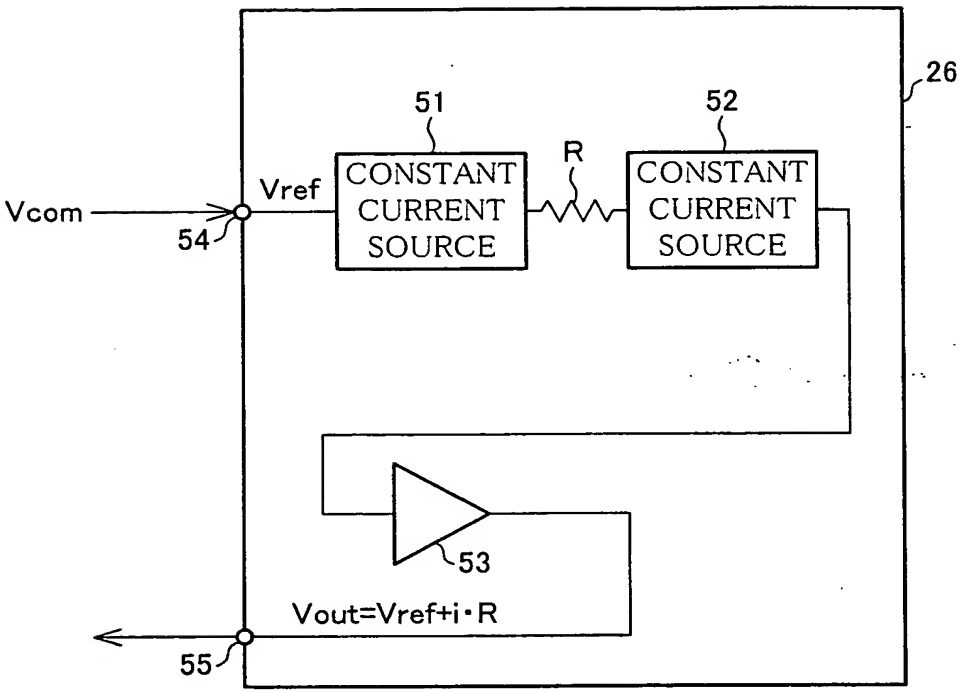

26
51
52
R
Vref
CONSTANT CURRENT SOURCE
CONSTANT CURRENT SOURCE
Vcom
54
53
Vout=Vref+i·R
55

FIG. 8 (a)

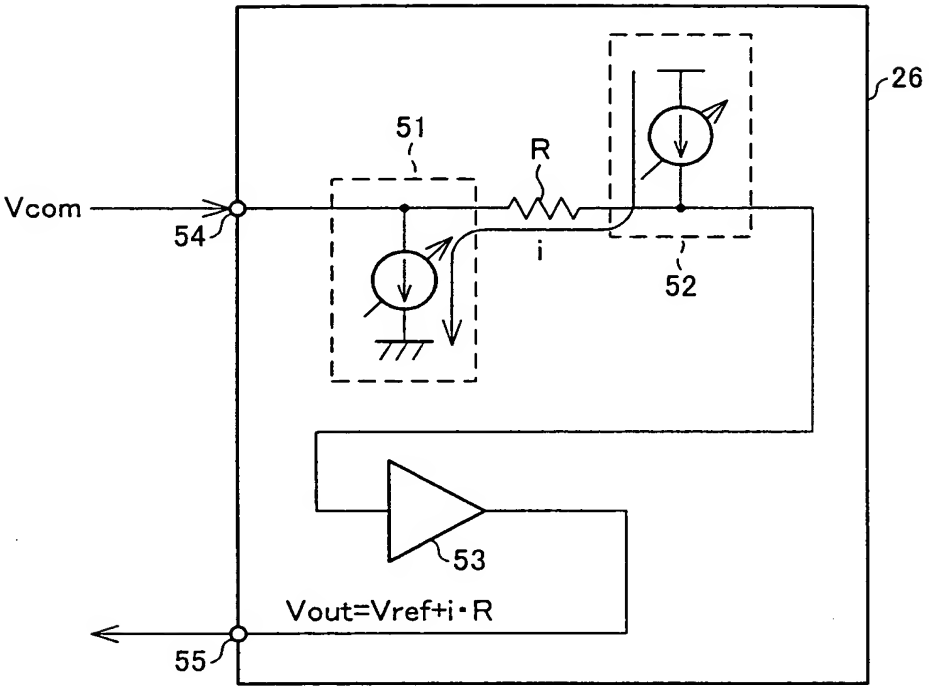

26
51
R
Vcom
54
i
52
53
Vout=Vref+i・R
55

FIG. 8 (b)

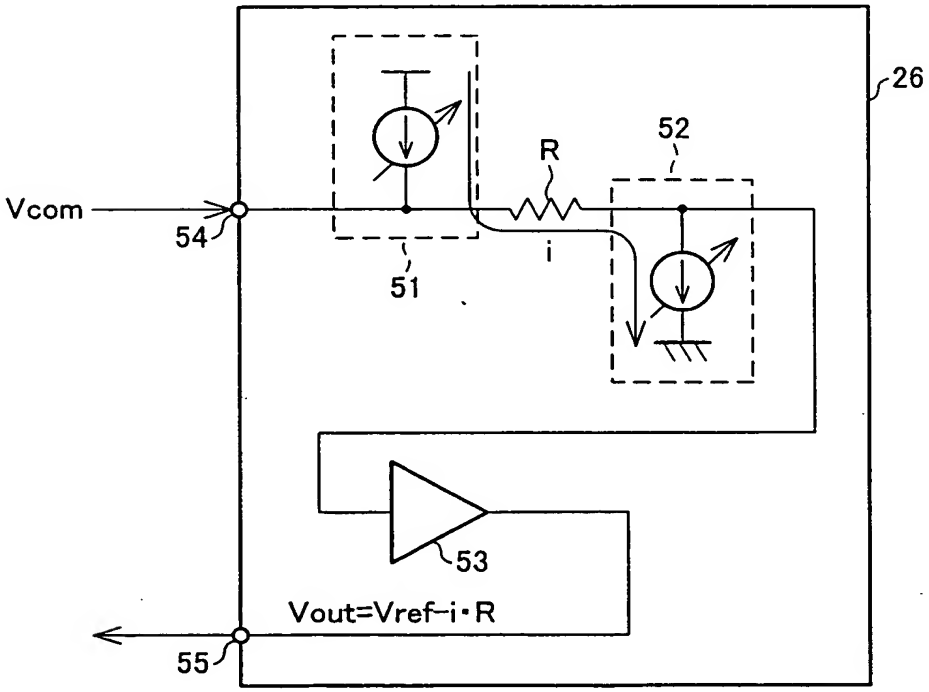

26
52
R
Vcom
54
i
51
53
Vout=Vref−i・R
55

FIG. 9

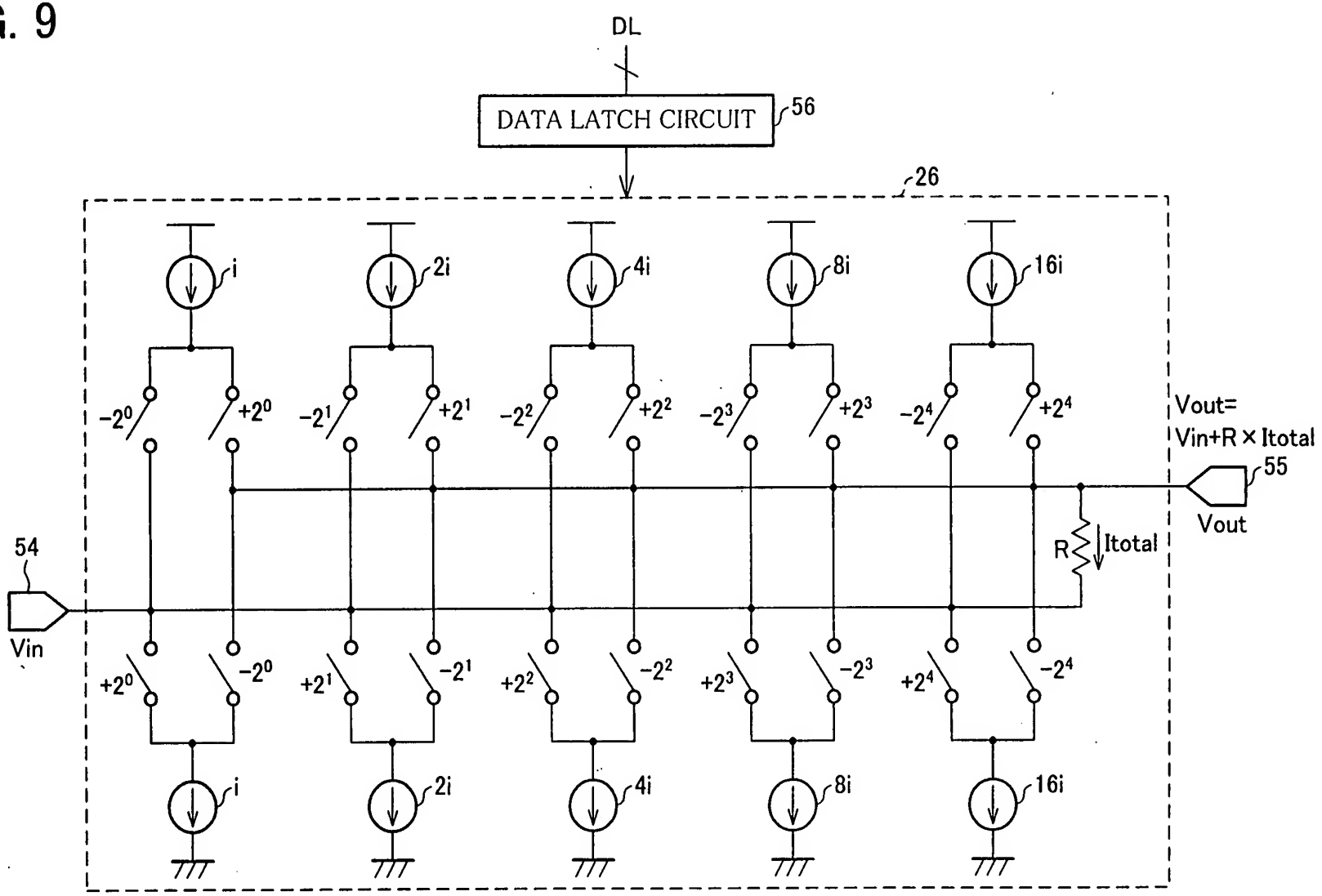

DL
DATA LATCH CIRCUIT
56
26
i
2i
4i
8i
16i
-2^0
$+2^0$
-2^1
$+2^1$
-2^2
$+2^2$
-2^3
$+2^3$
-2^4
$+2^4$
Vout=
Vin+R × Itotal
55
Vout
R
Itotal
54
Vin

FIG. 10

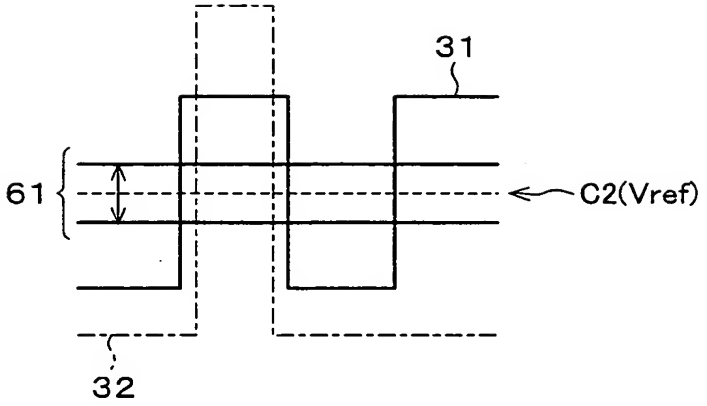


FIG. 11

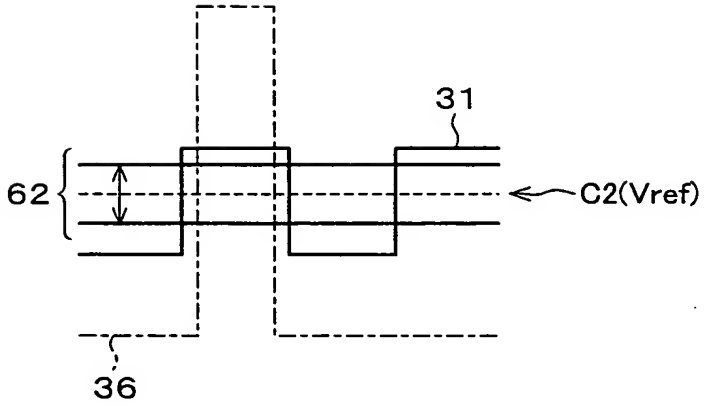


FIG. 12

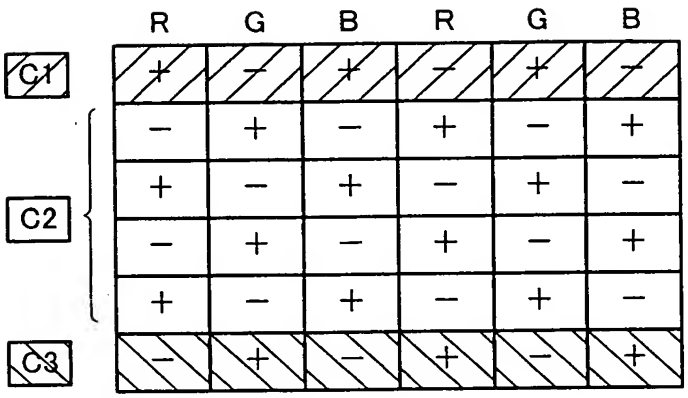


FIG. 13

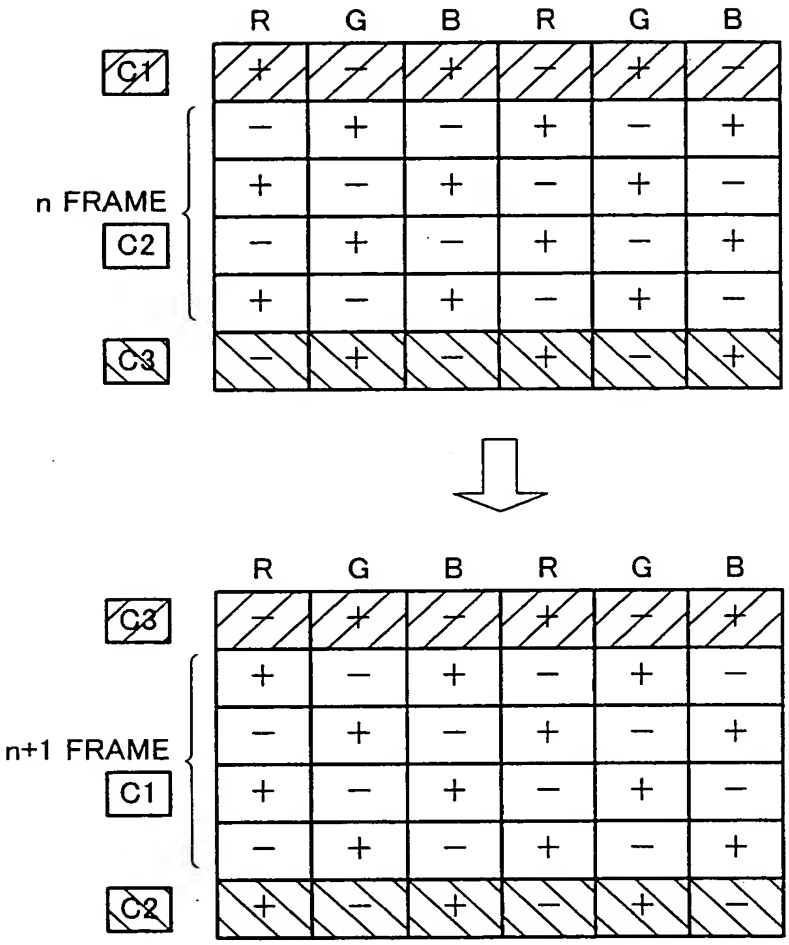

R G B R G B
C1
n FRAME
C2
C3
R G B R G B
C3
n+1 FRAME
C1
C2

FIG. 14

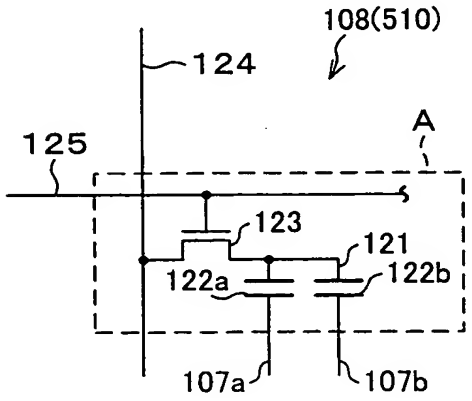

108(510)
124
A
125
123
121
122a
122b
107a
107b

FIG. 15

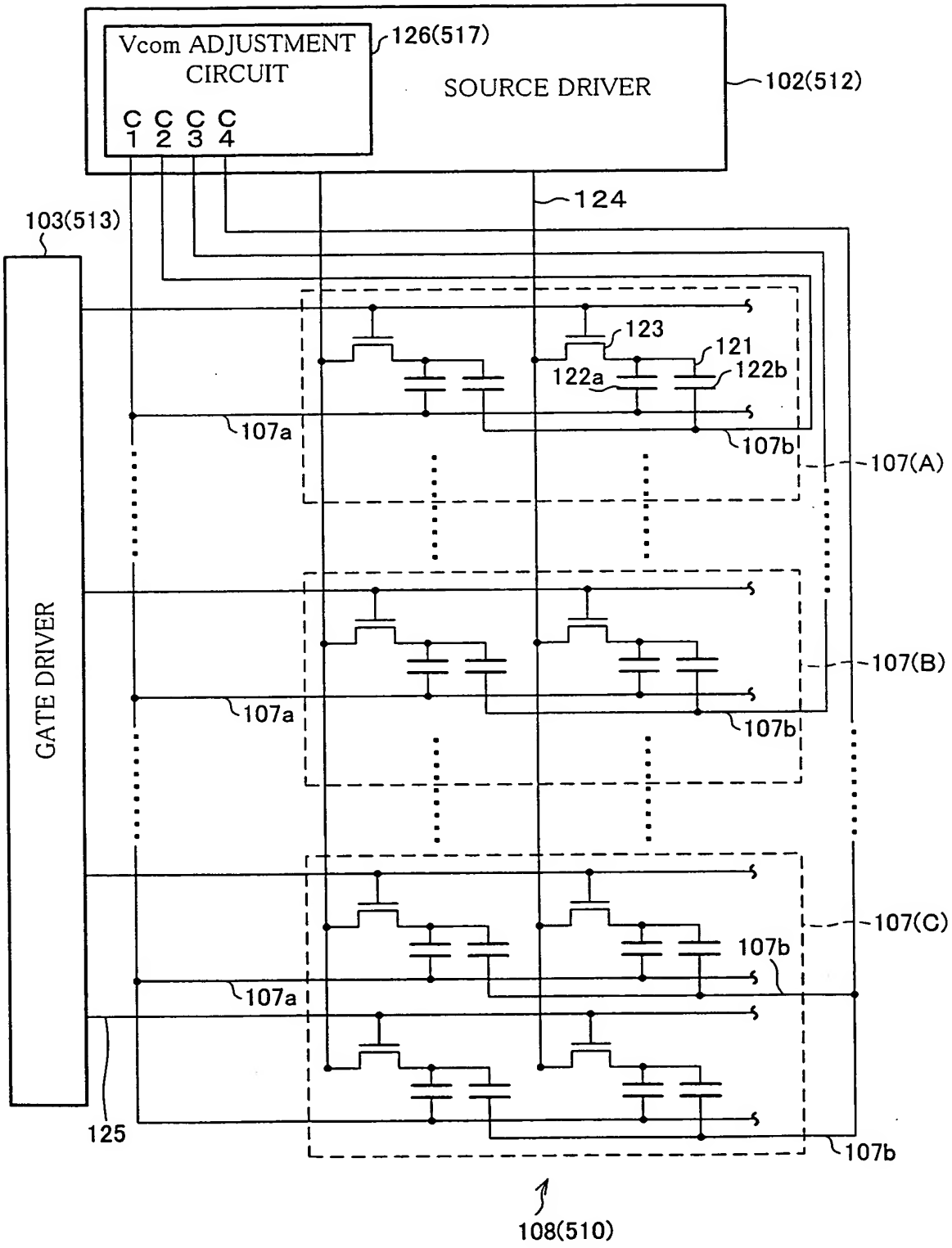
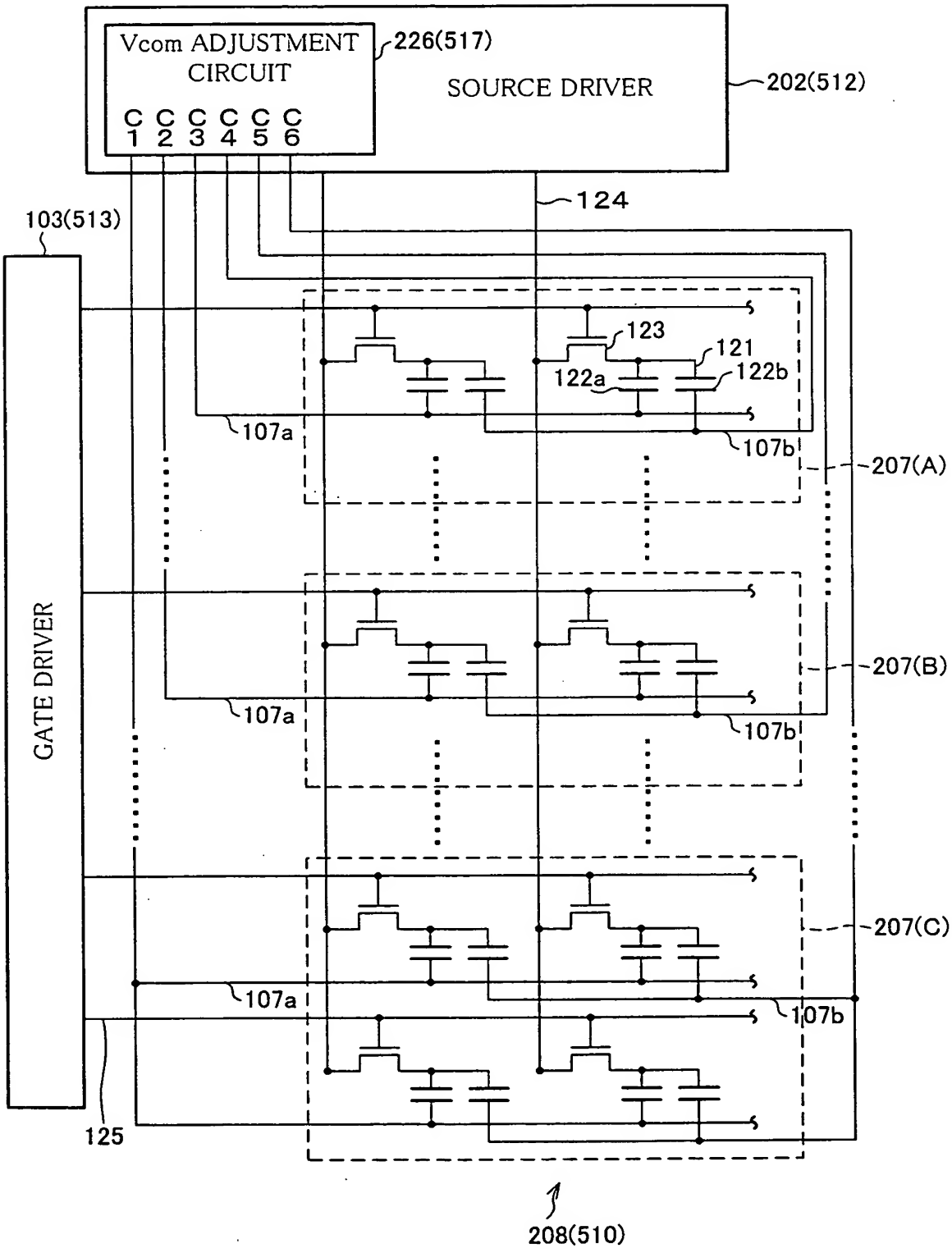

Vcom ADJUSTMENT CIRCUIT
126(517)
SOURCE DRIVER
102(512)
C 1
C 2
C 3
C 4
124
103(513)
GATE DRIVER
123
121
122a
122b
107a
107b
107(A)
107(B)
107(C)
125
108(510)

FIG. 16


Vcom ADJUSTMENT CIRCUIT
226(517)
SOURCE DRIVER
202(512)
C1 C2 C3 C4 C5 C6
124
103(513)
GATE DRIVER
123
121
122a
122b
107a
107b
207(A)
207(B)
207(C)
125
208(510)

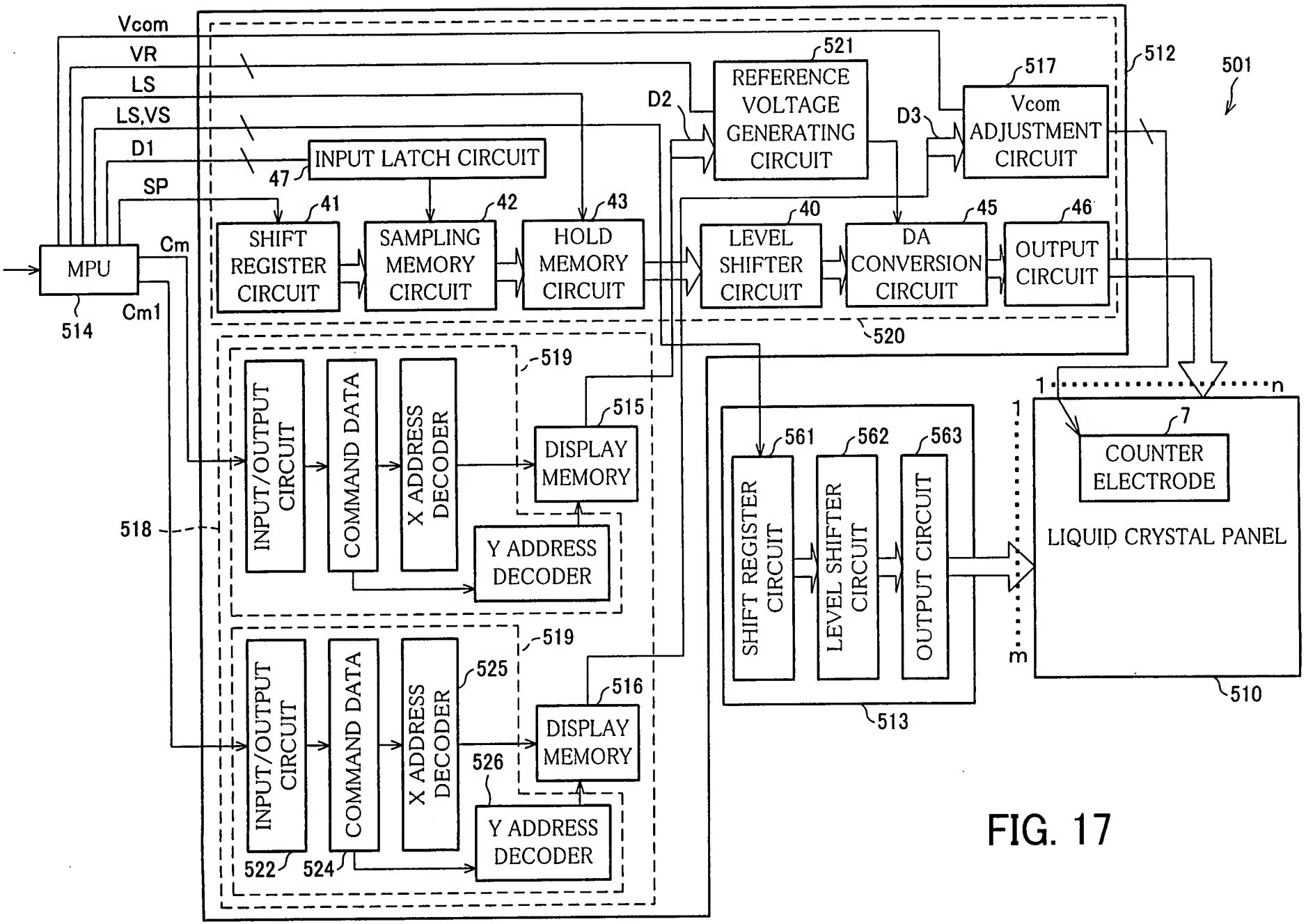

Vcom
VR
LS
LS,VS
D1
SP
Cm
Cm1
MPU
514
INPUT LATCH CIRCUIT
47
SHIFT REGISTER CIRCUIT
41
SAMPLING MEMORY CIRCUIT
42
HOLD MEMORY CIRCUIT
43
REFERENCE VOLTAGE GENERATING CIRCUIT
521
D2
D3
Vcom ADJUSTMENT CIRCUIT
517
512
501
LEVEL SHIFTER CIRCUIT
40
DA CONVERSION CIRCUIT
45
OUTPUT CIRCUIT
46
520
519
INPUT/OUTPUT CIRCUIT
COMMAND DATA
X ADDRESS DECODER
DISPLAY MEMORY
515
Y ADDRESS DECODER
518
519
INPUT/OUTPUT CIRCUIT
COMMAND DATA
X ADDRESS DECODER
525
DISPLAY MEMORY
516
526
Y ADDRESS DECODER
522
524
SHIFT REGISTER CIRCUIT
561
LEVEL SHIFTER CIRCUIT
562
OUTPUT CIRCUIT
563
513
1
n
1
3
COUNTER ELECTRODE
7
LIQUID CRYSTAL PANEL
510

FIG. 17

FIG. 18

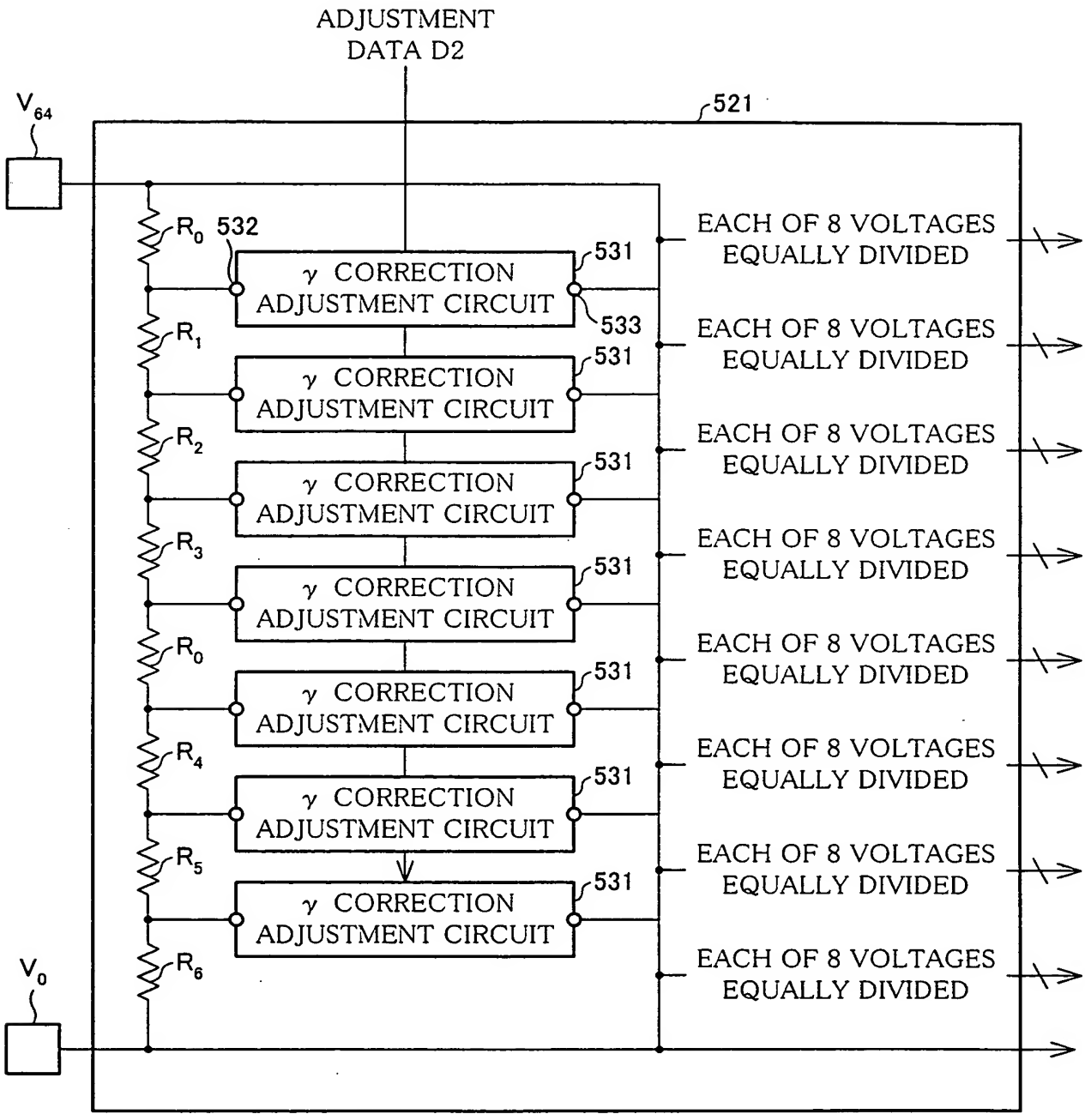

ADJUSTMENT DATA D2
521
V_{64}
V_0
R_0
R_1
R_2
R_3
R_0
R_4
R_5
R_6
532
531
533
γ CORRECTION ADJUSTMENT CIRCUIT
EACH OF 8 VOLTAGES EQUALLY DIVIDED

FIG. 19

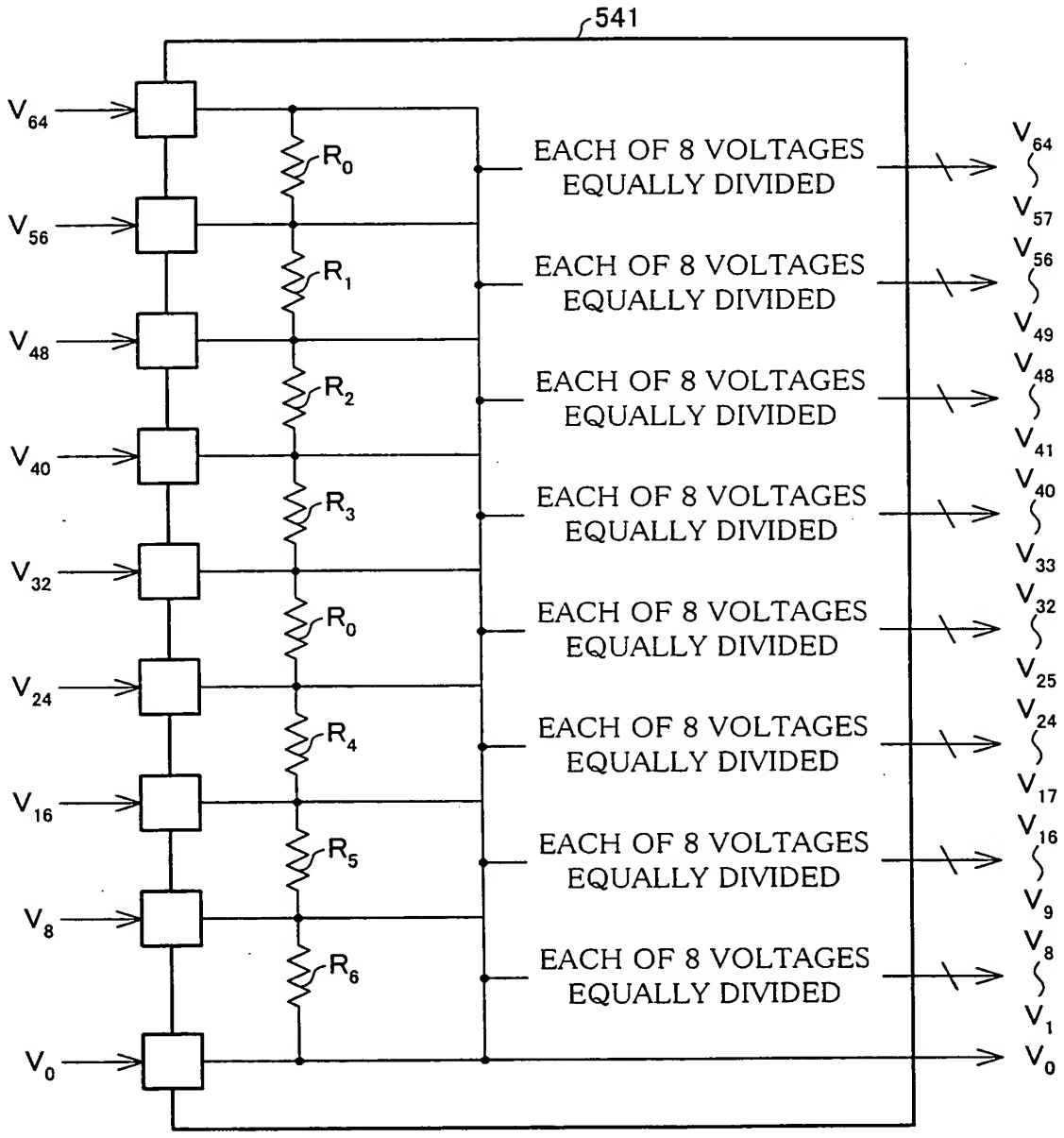

541
V_{64}
V_{56}
V_{48}
V_{40}
V_{32}
V_{24}
V_{16}
V_8
V_0
R_0
R_1
R_2
R_3
R_0
R_4
R_5
R_6
EACH OF 8 VOLTAGES EQUALLY DIVIDED
EACH OF 8 VOLTAGES EQUALLY DIVIDED
EACH OF 8 VOLTAGES EQUALLY DIVIDED
EACH OF 8 VOLTAGES EQUALLY DIVIDED
EACH OF 8 VOLTAGES EQUALLY DIVIDED
EACH OF 8 VOLTAGES EQUALLY DIVIDED
EACH OF 8 VOLTAGES EQUALLY DIVIDED
V_{64}
V_{57}
V_{56}
V_{49}
V_{48}
V_{41}
V_{40}
V_{33}
V_{32}
V_{25}
V_{24}
V_{17}
V_{16}
V_9
V_8
V_1
V_0

FIG. 20

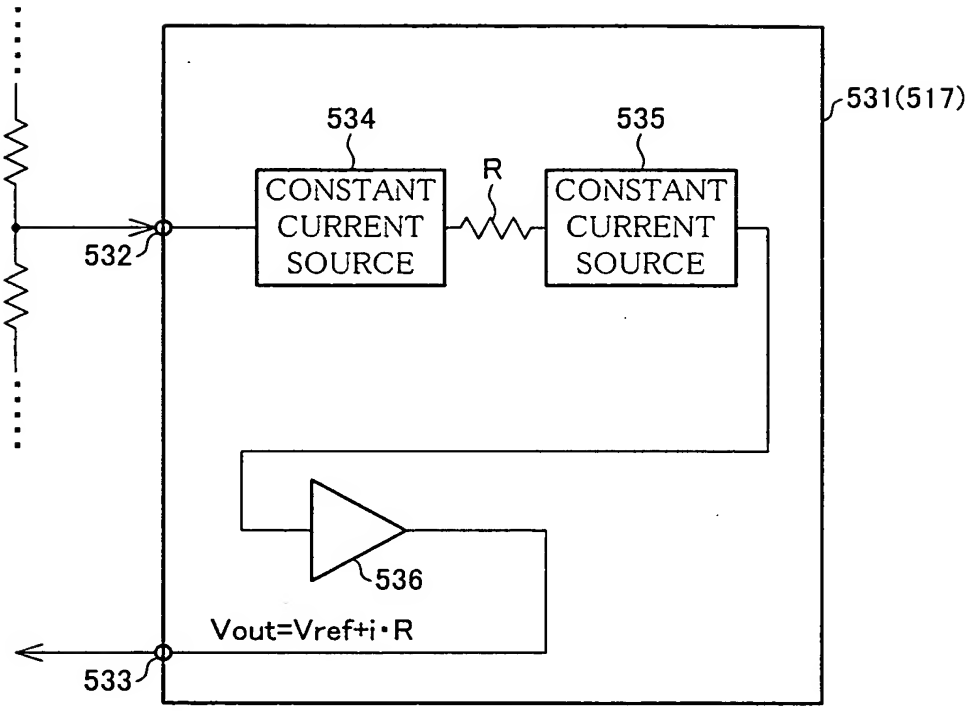

531(517)
534
535
R
CONSTANT CURRENT SOURCE
CONSTANT CURRENT SOURCE
532
536
Vout=Vref+i・R
533

FIG. 21 (a)

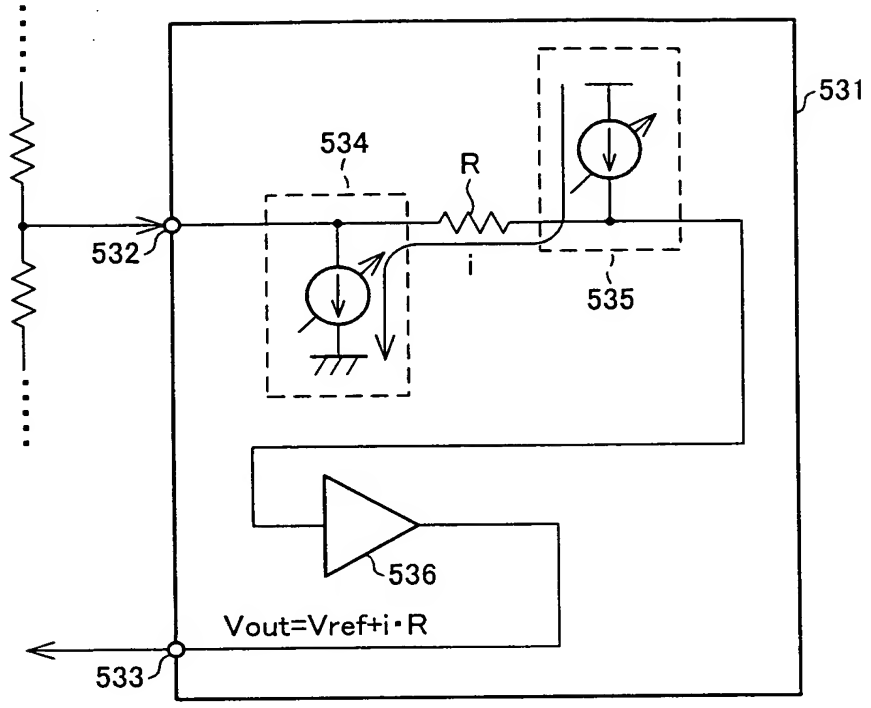


FIG. 21 (b)

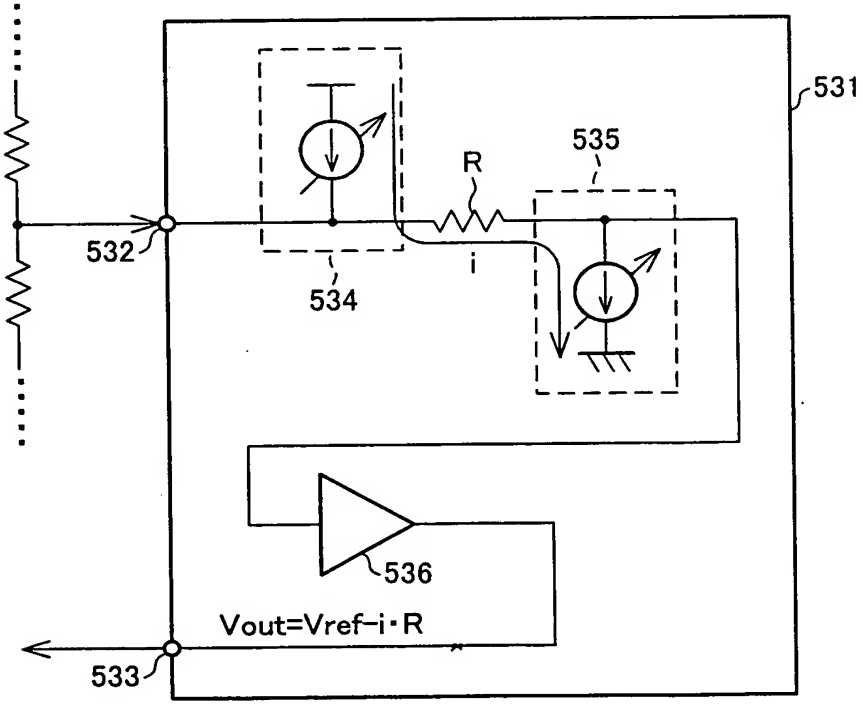


FIG. 22

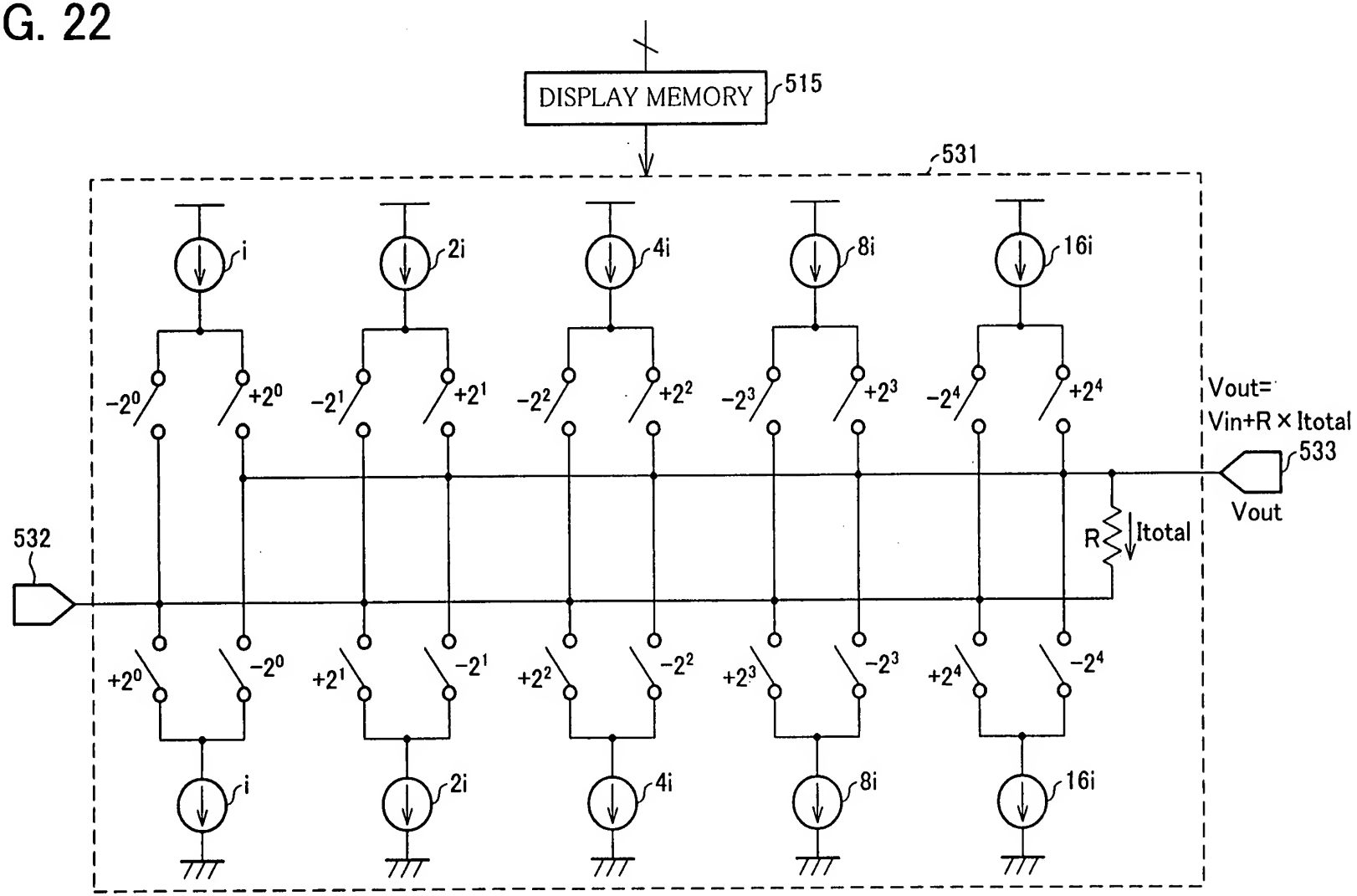

DISPLAY MEMORY
515
531
i
2i
4i
8i
16i
-2^0
$+2^0$
-2^1
$+2^1$
-2^2
$+2^2$
-2^3
$+2^3$
-2^4
$+2^4$
Vout=
Vin+R × Itotal
533
Vout
R
Itotal
532

FIG. 23

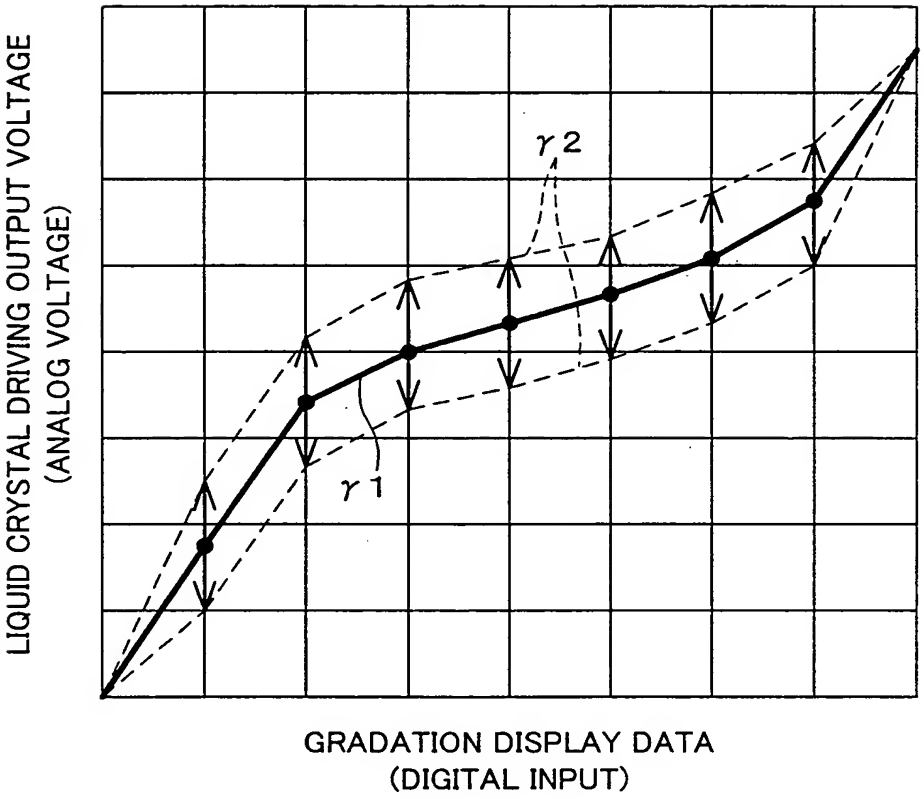

LIQUID CRYSTAL DRIVING OUTPUT VOLTAGE
(ANALOG VOLTAGE)
γ2
γ1
GRADATION DISPLAY DATA
(DIGITAL INPUT)

FIG. 24

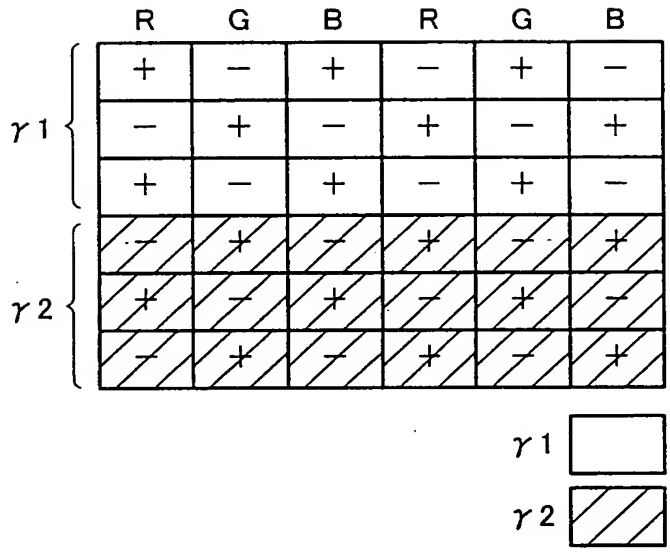


FIG. 25

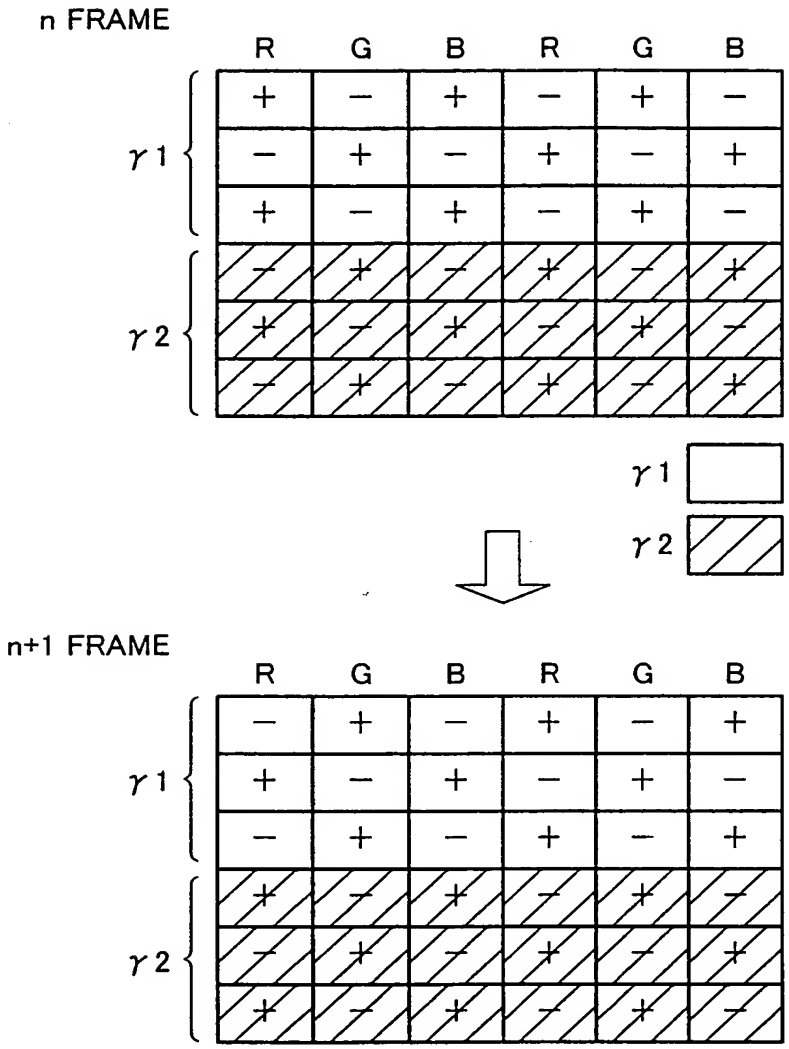


FIG. 26

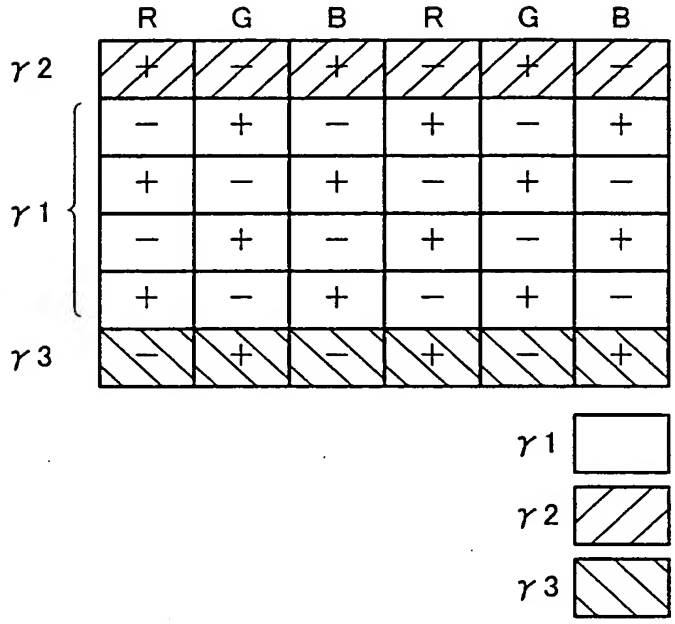


FIG. 27

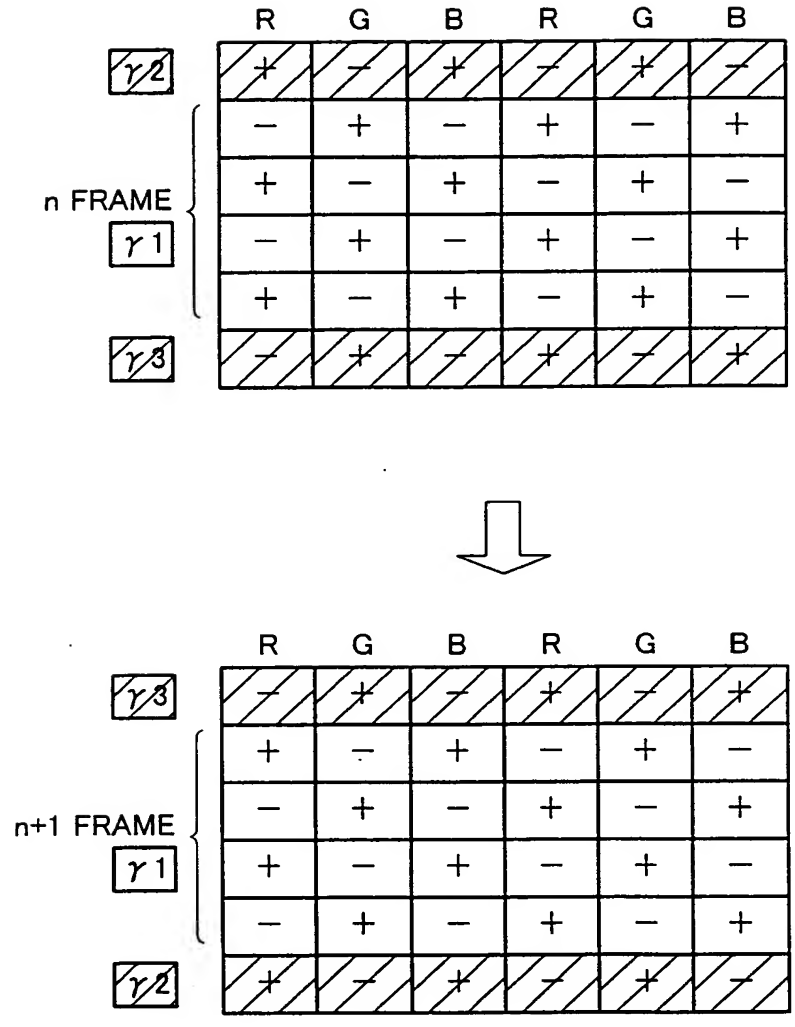


FIG. 28

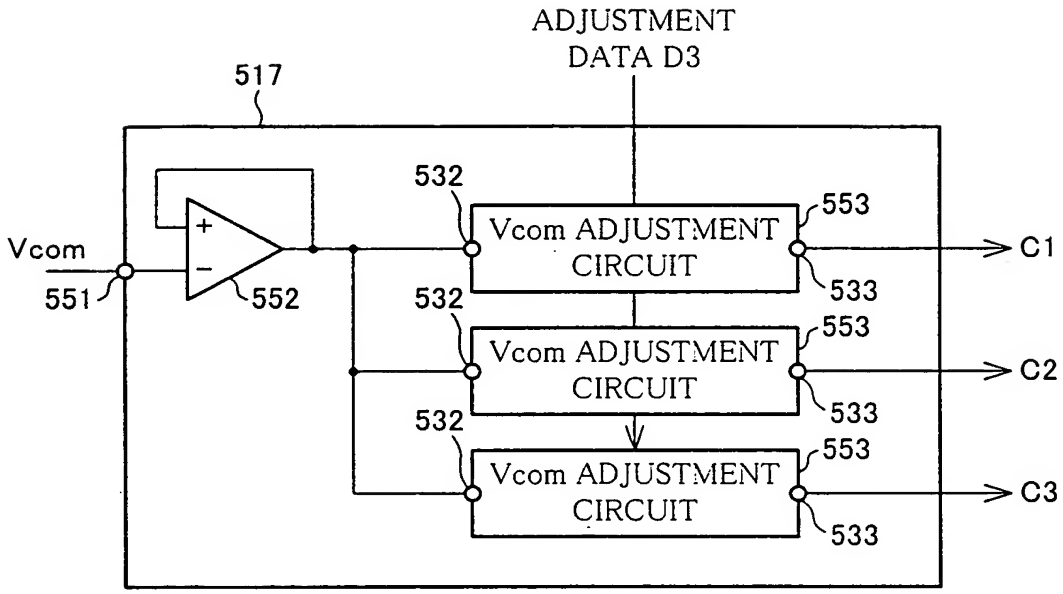
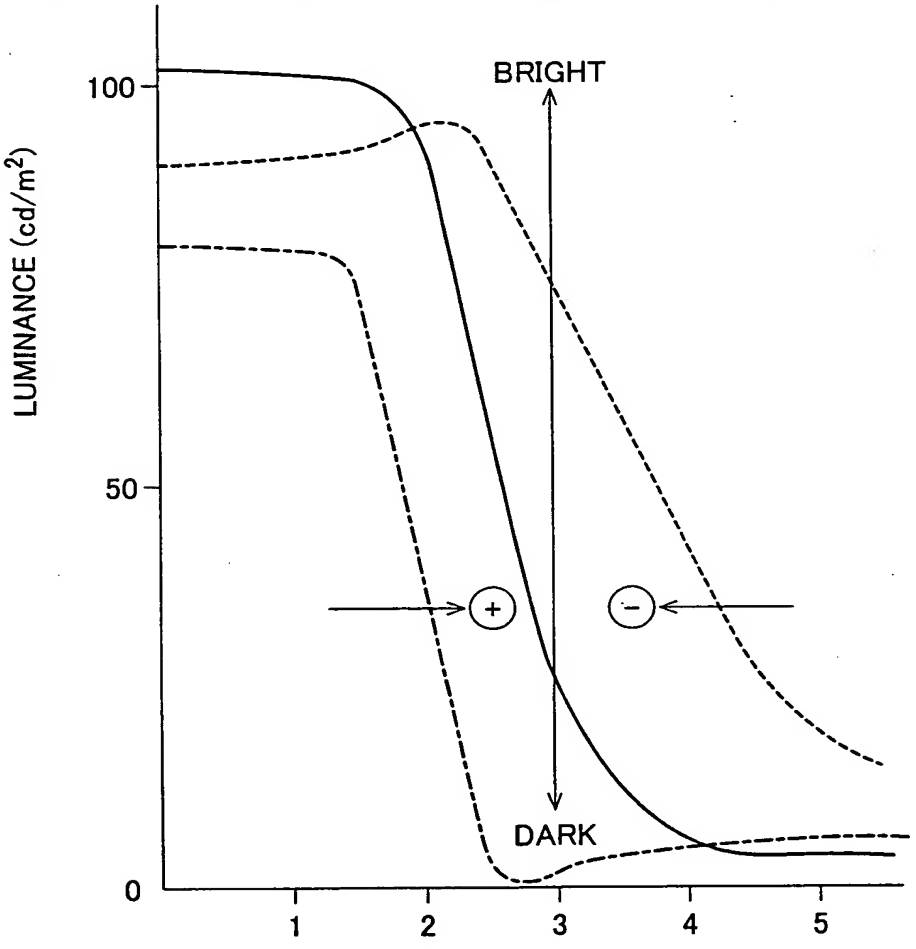

ADJUSTMENT
DATA D3
517
532
553
Vcom ADJUSTMENT
CIRCUIT
533
C1
Vcom
551
552
C2
C3

FIG. 29

GRAPH SHOWING A RELATIONSHIP BETWEEN LUMINANCE OF A SINGLE PIXEL OF A LIQUID CRYSTAL PANEL AND AN ANGULAR POSITION IN VIEWING



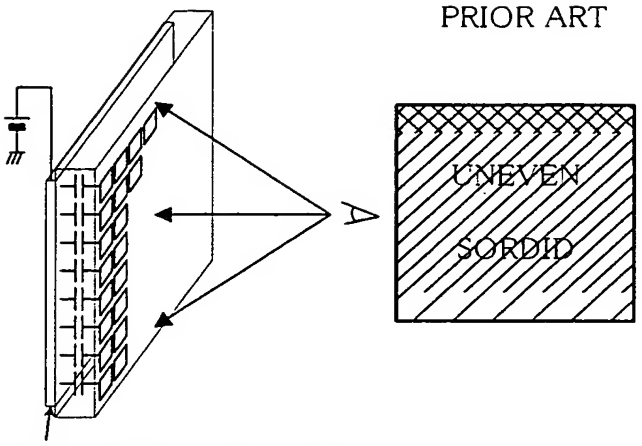
VOLTAGE APPLIED TO A LIQUID CRYSTAL CELL (V)

-------- ϕ =-30° (VIEWING DOWNWARD)

——— ϕ =0° (VIEWING IN A FRONT DIRECTION)

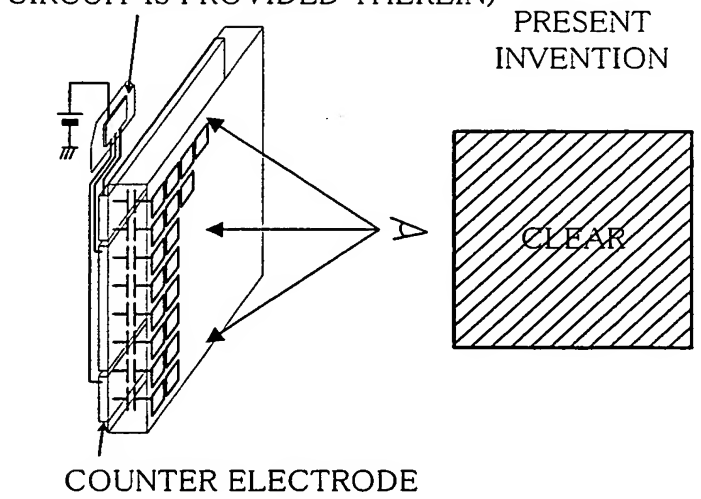
- - - - - - ϕ =+30° (VIEWING UPWARD)

FIG. 30 (a)



In a case of a large screen panel, an angular position in viewing varies depending on whether an image is viewed from an upper direction or a lower direction, so that the image does not seem uniformed even when the image is uniformly displayed.

FIG. 30 (b)



A plurality of counter electrodes are prepared and are independently controlled, thereby controlling the display so that an image seems uniformed when viewed from an upper direction or a lower direction.

FIG. 30 (c)

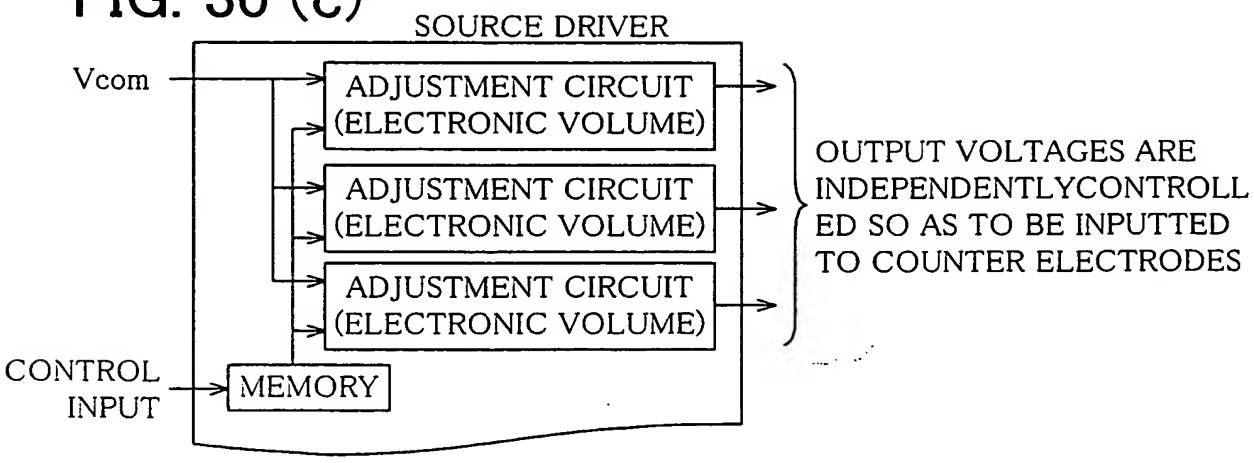


FIG. 31

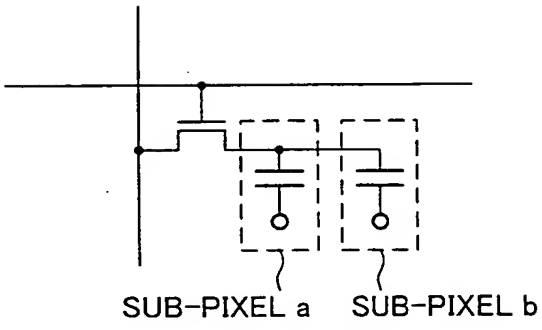


FIG. 32 (a)

LIGHT INTENSITY OF A PIXEL/SIGNAL VOLTAGE CHARACTERISTIC(θ =40°)

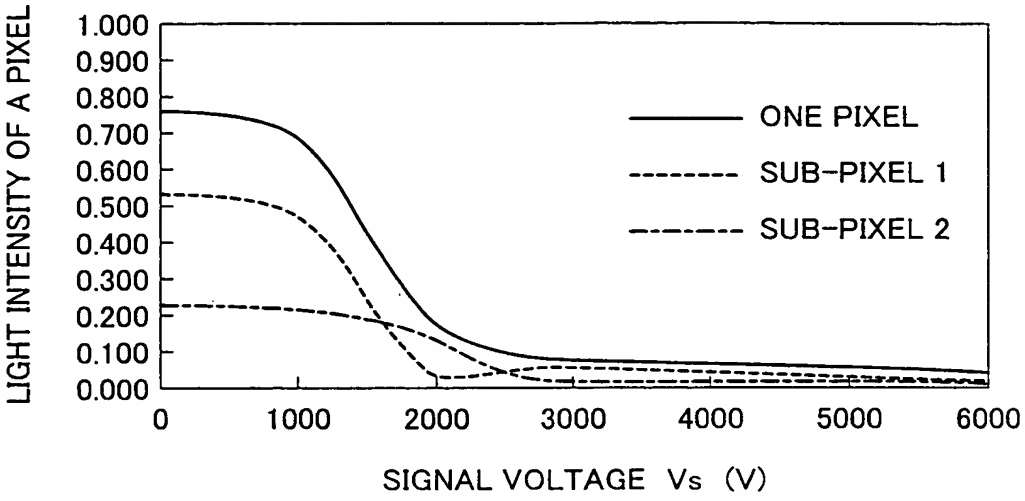


FIG. 32 (b)

LIGHT INTENSITY OF A PIXEL/SIGNAL VOLTAGE CHARACTERISTIC(θ =40°)

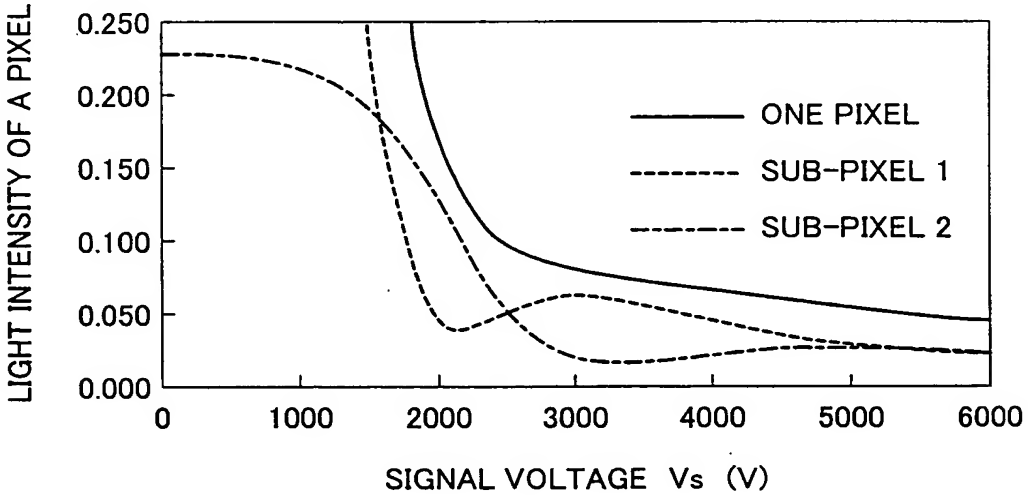


FIG. 33 (a)

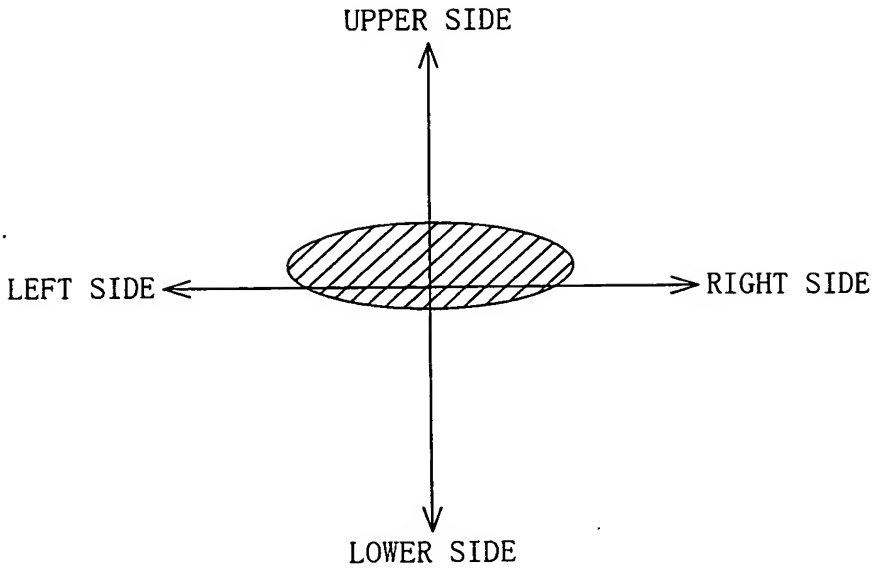


FIG. 33 (b)

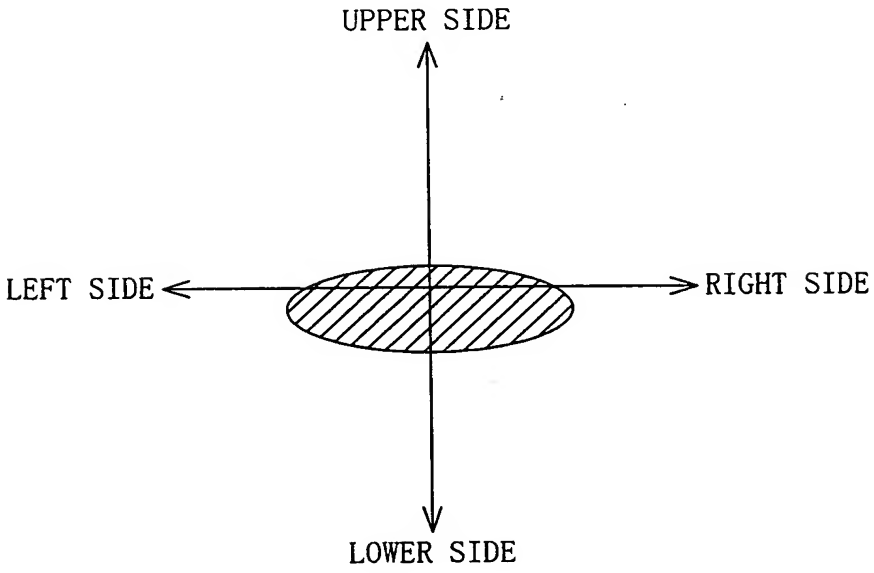


FIG. 34

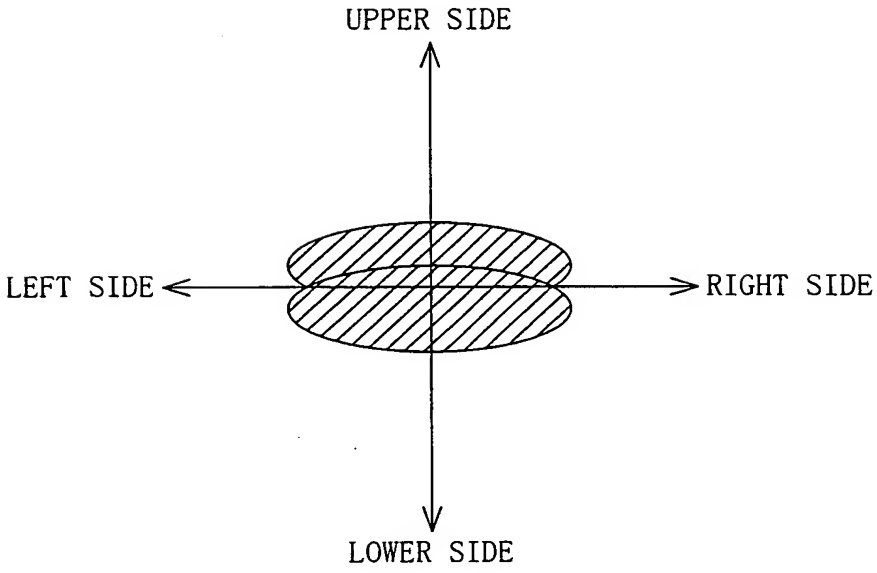
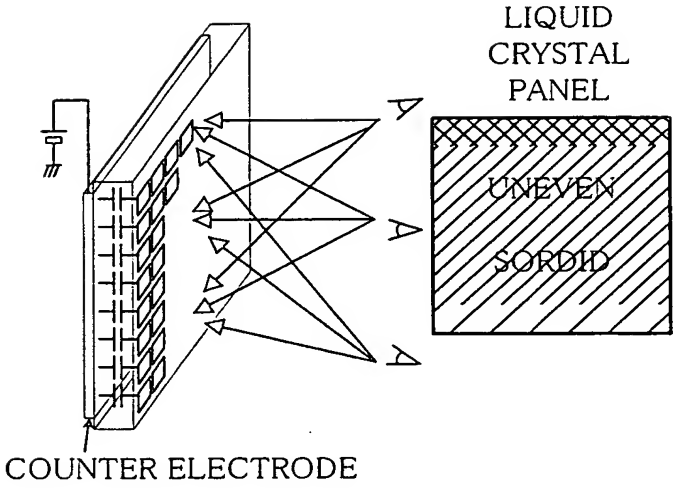
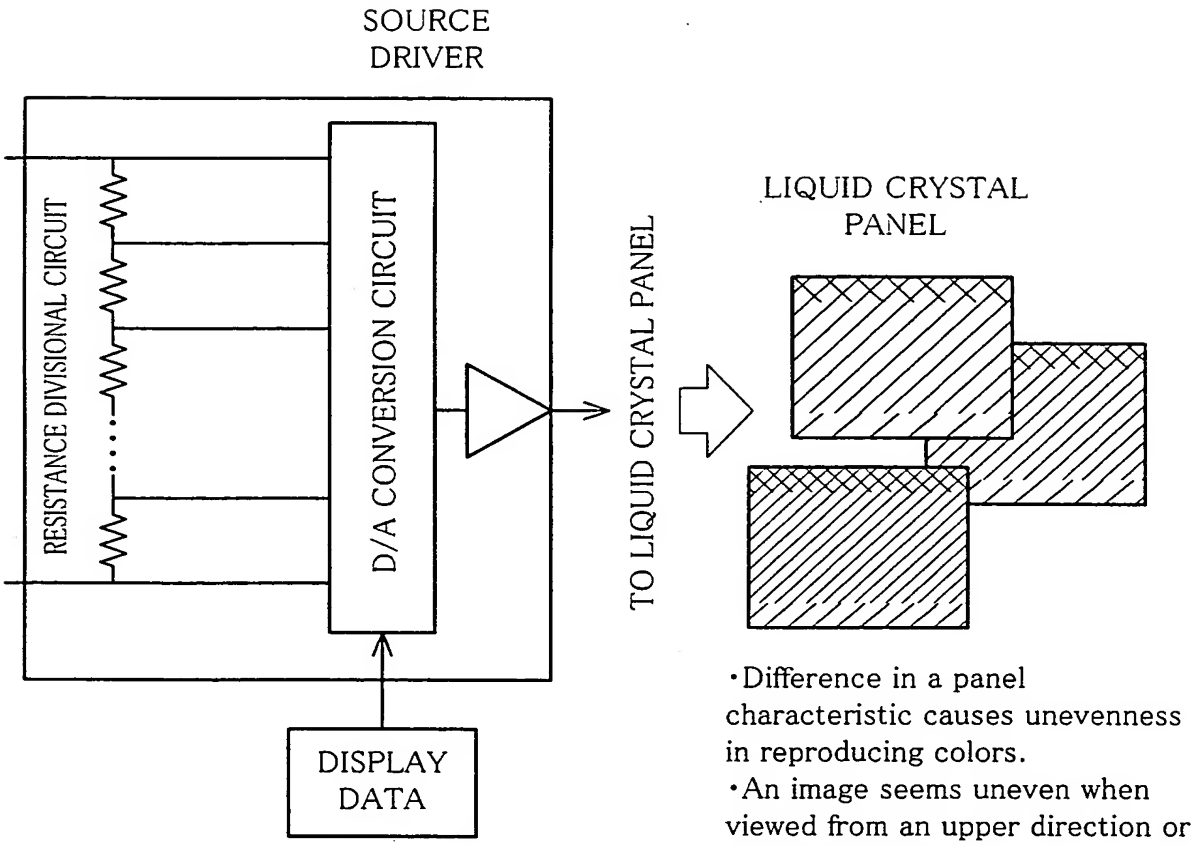


FIG. 35



In a case of a large screen panel, an angular position in viewing varies depending on whether an image is viewed from an upper direction or a lower direction, so that the image does not seem uniformed even when the image is uniformly displayed. Further, difference in a panel characteristic causes unevenness in reproducing colors.

FIG. 36



- Difference in a panel characteristic causes unevenness in reproducing colors.
- An image seems uneven when viewed from an upper direction or a lower direction.

FIG. 37

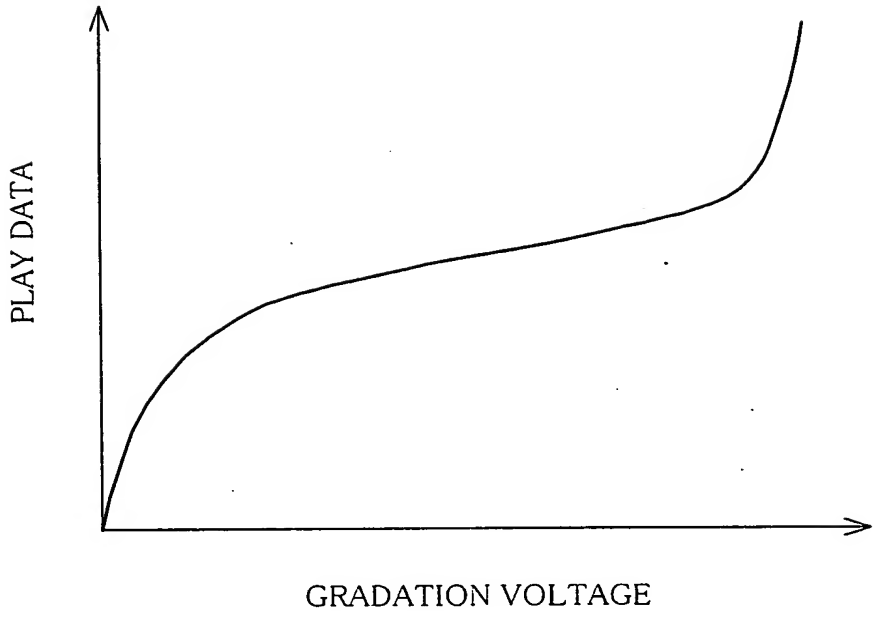
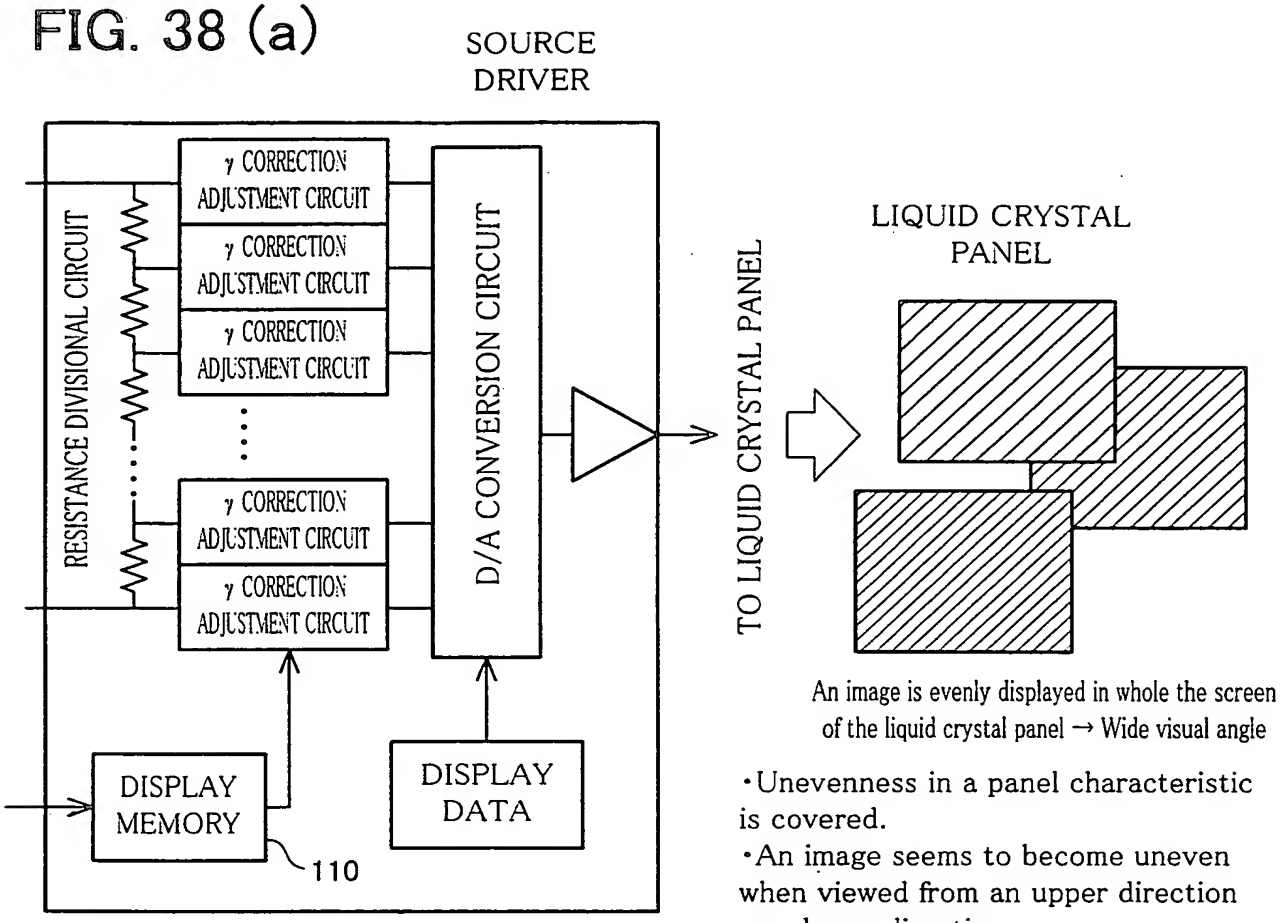


FIG. 38 (a)



An image is evenly displayed in whole the screen of the liquid crystal panel → Wide visual angle

- Unevenness in a panel characteristic is covered.
- An image seems to become uneven when viewed from an upper direction or a lower direction
- It is not necessary to perform a special rubbing process

FIG. 38 (b)

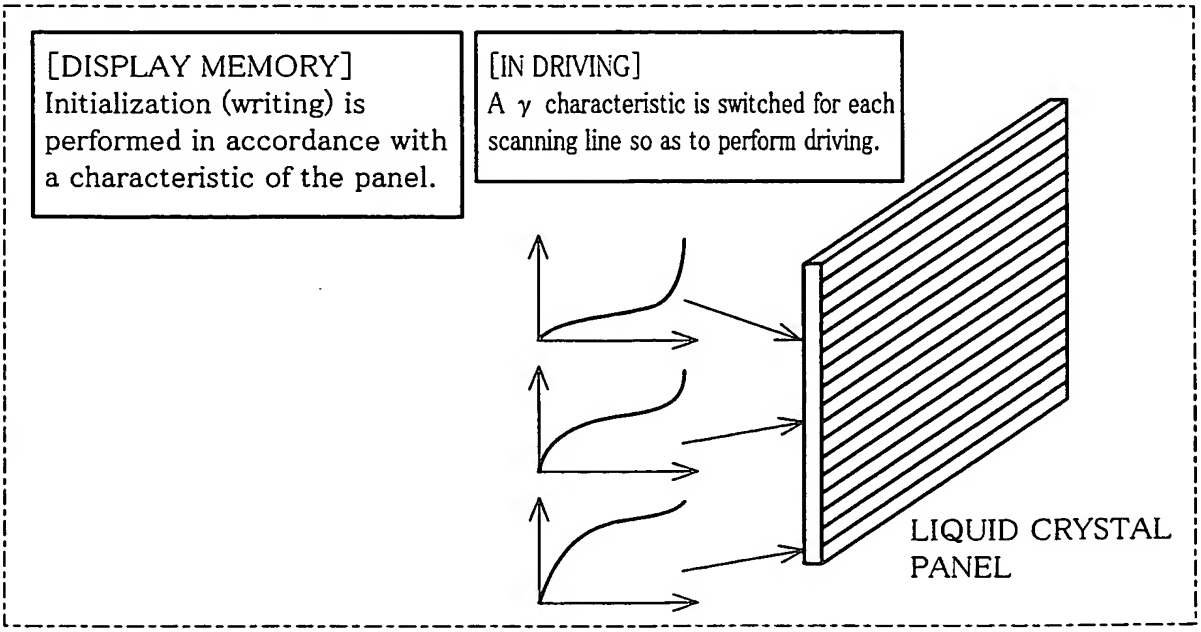


FIG. 39

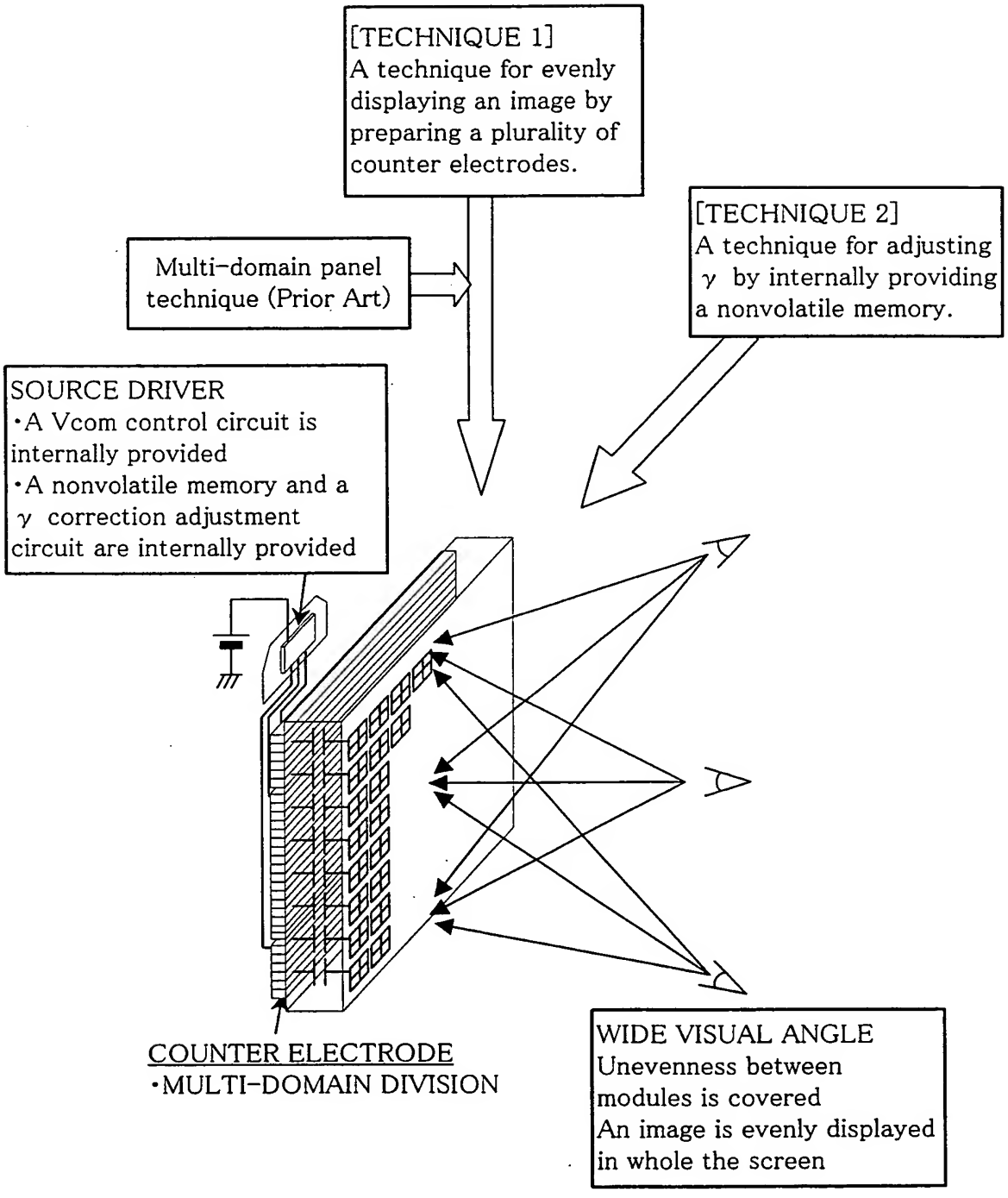

[TECHNIQUE 1]
A technique for evenly displaying an image by preparing a plurality of counter electrodes.
[TECHNIQUE 2]
A technique for adjusting γ by internally providing a nonvolatile memory.
Multi-domain panel technique (Prior Art)
SOURCE DRIVER
•A Vcom control circuit is internally provided
•A nonvolatile memory and a γ correction adjustment circuit are internally provided
COUNTER ELECTRODE
•MULTI-DOMAIN DIVISION
WIDE VISUAL ANGLE
Unevenness between modules is covered
An image is evenly displayed in whole the screen

FIG. 40

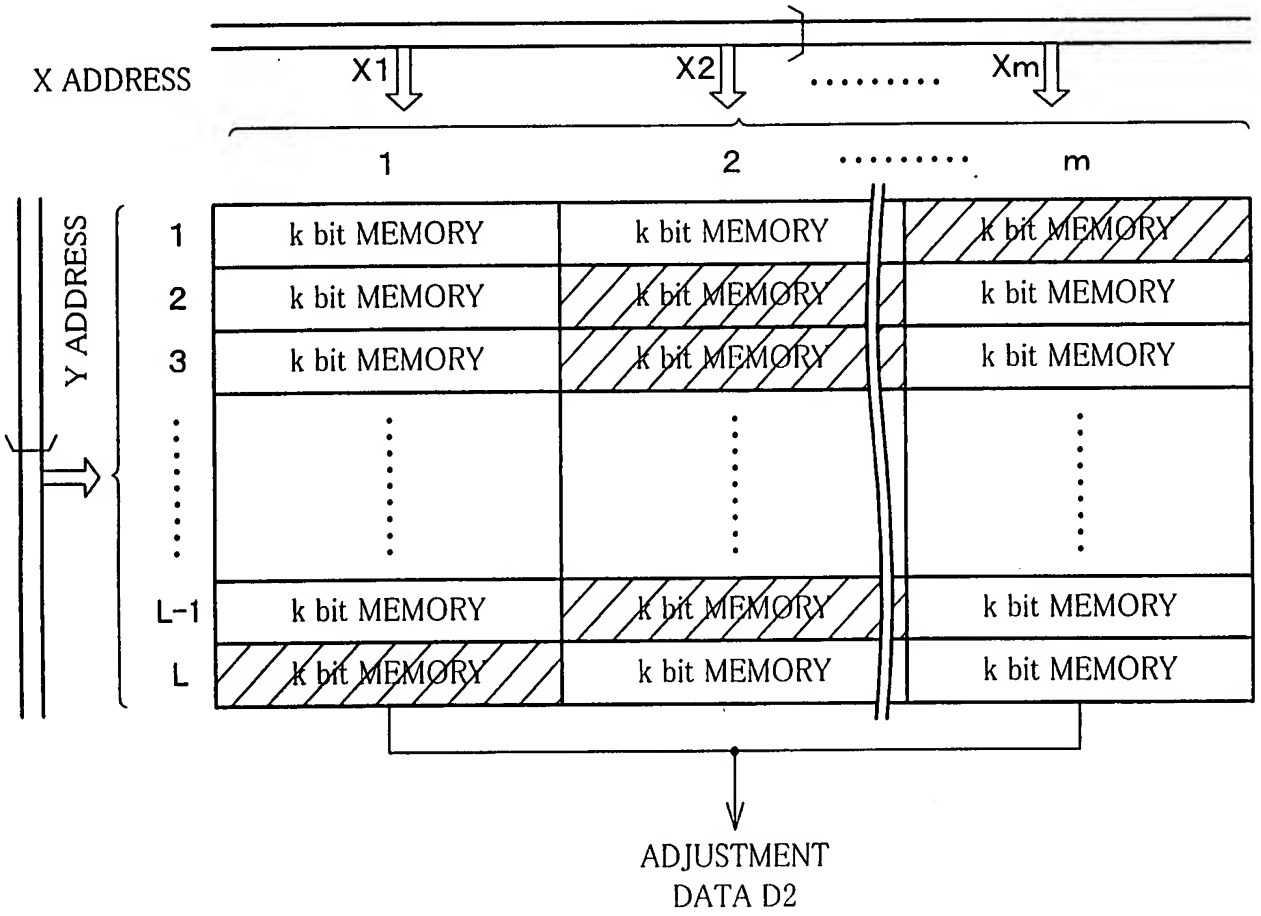

X ADDRESS
X1
X2
Xm
1
2
m
Y ADDRESS
1
2
3
L-1
L
k bit MEMORY
ADJUSTMENT
DATA D2

FIG. 41

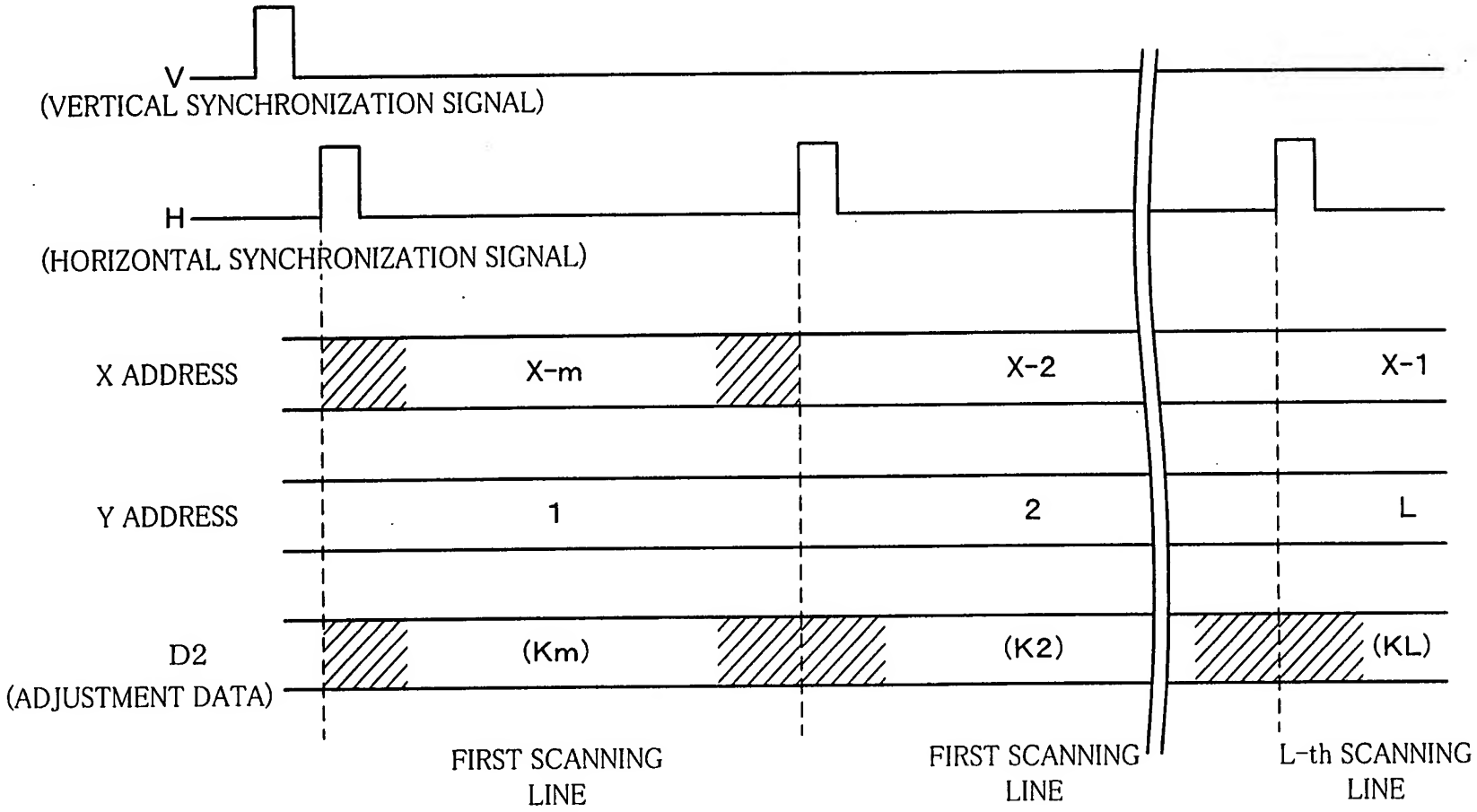
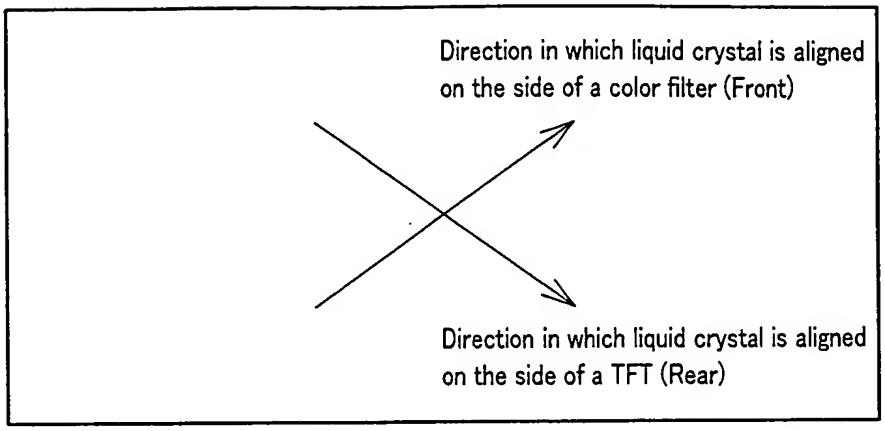
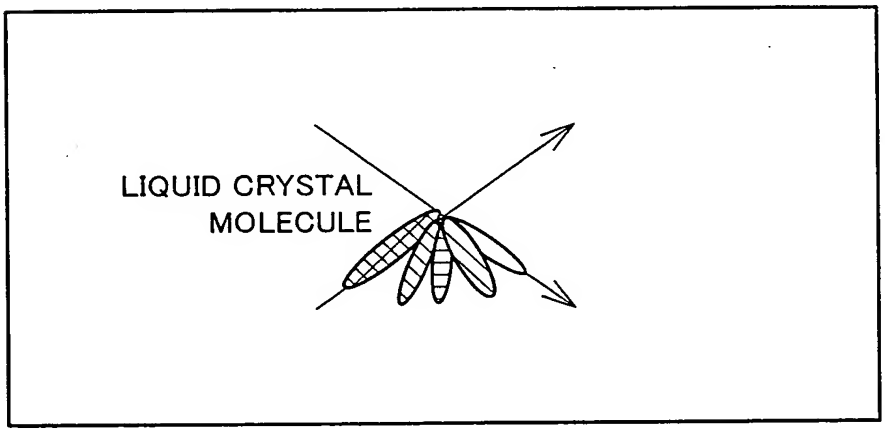

V
(VERTICAL SYNCHRONIZATION SIGNAL)
H
(HORIZONTAL SYNCHRONIZATION SIGNAL)
X ADDRESS
X-m
X-2
X-1
Y ADDRESS
1
2
L
D2
(ADJUSTMENT DATA)
(Km)
(K2)
(KL)
FIRST SCANNING LINE
FIRST SCANNING LINE
L-th SCANNING LINE

FIG. 42 (a)



RUBBING DIRECTION

FIG. 42 (b)



LIQUID CRYSTAL ALIGNMENT (UPPER SURFACE)

FIG. 42 (c)

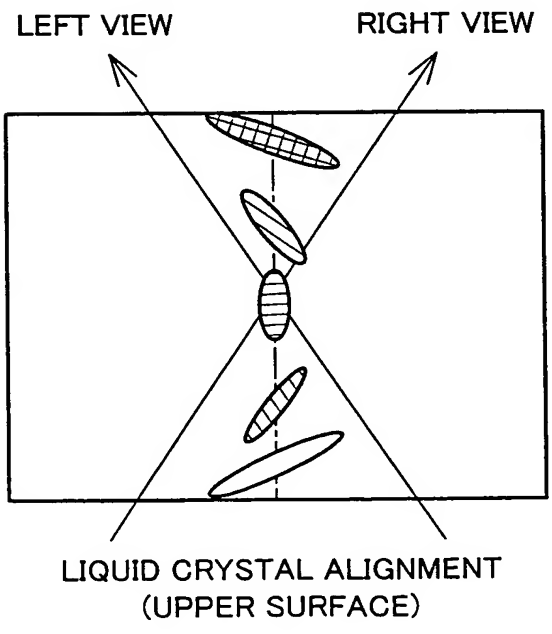


FIG. 42 (d)

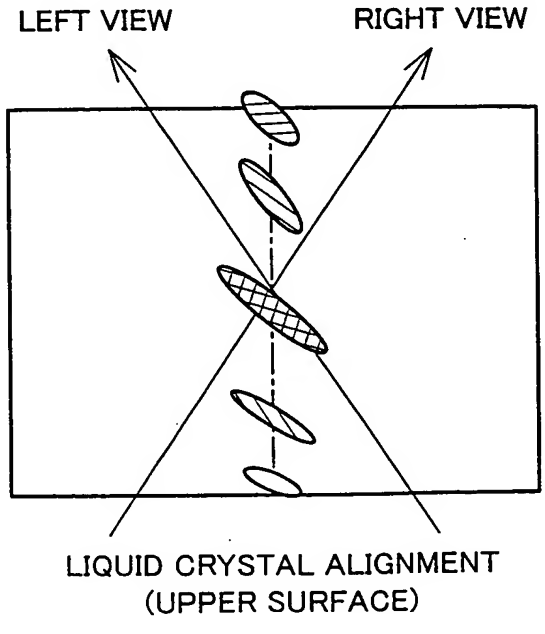
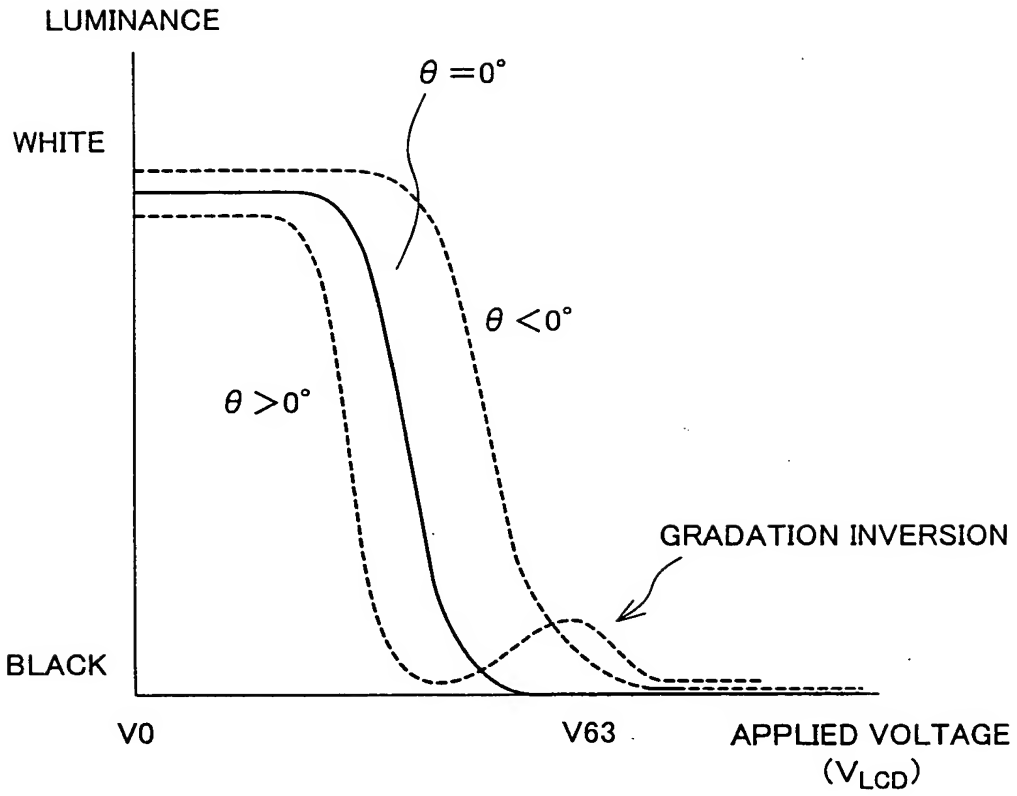


FIG. 43



VOLTAGE (V) APPLIED TO
A LIQUID CRYSTAL CELL